ACADEMIC YEAR 2020-2021

HUDSON VALLEY COMMUNITY COLLEGE
TROY, NEW YORK

COURSE OUTLINE

COURSE TITLE: Digital Electronics

COURSE SUBJECT AND NUMBER: ELET 210

DEPARTMENT: Applied Technologies

CREDIT HOURS: 4

CONTACT HOURS: 3 Lecture, 3 Lab

SEMESTER COURSE IS OFFERED: Fall

OFFERED DISTANCE LEARNING: Yes

PREREQUISITES: Yes **If yes, list prerequisite(s):** ELET 100- Electricity I

COREQUISITES: No **If yes, list corequisite(s):**

PREREQUISITE(S) OR COREQUISITE(S): No
TEXT(S): Digital Fundamentals – 10th Edition, Floyd, Prentice Hall, 2008
Digital Electronics Laboratory Manual, Michelen, Prentice Hall, 2000

LAB FEES: Yes

FINAL EXAM/FINAL PROJECT: Yes If yes, please specify: Final Exam

ORIGINAL SUBMISSION DATE: 2003

CURRICULUM COMMITTEE APPROVED REVISION DATE: Fall 2005

PREPARED BY: Abraham Michelen

COURSE DESCRIPTION: An introductory course in digital systems. The topics covered include: Number Systems, Boolean Algebra, Logic Gates, logic simplification, implementation and analysis of digital system, Flip-flops, Counters, Mux/Demux, Adders.

ACTIVITIES AND ASSIGNMENTS: Activities and exercises will include, but are not limited to, in-class assignments, labs, tests, and a final exam.

GRADE COMPUTATION: (In general terms as defined by college policy. Specifics, including Z grade, will be defined on the instructor's syllabus).

Labs, tests and assignments: 75%
Final exam: 25%

ADA COMPLIANCE: In compliance with the Americans with Disabilities Act of 1990 and with Section 504 of the Rehabilitation Act, Hudson Valley Community College is committed to ensuring educational access and accommodations for all its registered students, in order to fully participate in programs and course activities or to meet course requirements. Hudson Valley Community College's students with documented disabilities and medical conditions are encouraged to access these services by registering with the Center for Access and Assistive Technology to discuss their particular needs for accommodations. For information or an appointment contact the Center for Access and Assistive Technology, located in room 130 of the Siek Campus Center or call 518-629-7154/TDD:518-629-7596.

STUDENT BEHAVIORAL OBJECTIVES:
Students will be able to:
1. Demonstrate understanding of Pulse Nomenclature and means of calculating the values.
2. Demonstrate how to convert to and from Binary to Decimal or other radices.
3. Demonstrate ability to determine the trust table and vice versa given a Boolean function.
4. Demonstrate addition & subtraction of Binary & Hexadecial values using l's/2' or complement arithmetic.
5. Demonstrate the ability to simplify a complex Boolean function using mapping techniques.
6. Demonstrate the ability to reduce complexity using multiple output circuit methods.
7. Build a TTL half adder or full adder & demonstrate its use.
8. Design and build various types of Bi-stable Flip-Flops using 7400's or 7402's.
9. Use one type of Gate (NAND or NOR) to create the remaining basic Boolean functions.
10. Build a timer using a 555 IC.
11. Design an oscillator using a 555IC.
12. Design a counter for Binary or decimal count.
13. Connect the above decimal counter to a 7segment display.
14. Design a digital clock to time off of the 60 Hz line or a crystal oscillator.
15. Describe the function of multiplexers & demultiplexers and describe the operation of multiplexed systems.

TOPIC OUTLINE:
I. LOGIC LEVELS AND PULSE WAVEFORMS

- a. Pulse Nomenclature
- b. Pulse Parameter Definitions

II. NUMBER SYSTEMS

- a. Base Conversions
- b. Binary Number Systems
- c. Binary Related Number Systems
  1. Quaternary
  2. Octal

3. Hexadecimal

d. Binary Addition & Subtraction

e. Binary Coded Decimal (CD)

f. Digital Codes

III. DIGITAL BUILDING BLOCK

a. Logic Gates

1. Inverter

2. AND Gate

3. OR Gate

4. NOR Gate

5. NAND Gate

6. XOR Gate

7. XNOR Gate

b. Gate Propagation Delay Time

c. Power Dissipation

d. Noise Immunity

e. Unit Loading

f. Logic Gate Applications

g. Introduction to Programmable Logic Devices (PLD)

h. PLD Programmer Software

i. PLD Programmer Hardware

IV. BOOLEAN ALGEBRA

a. Boolean Laws

b. DeMorgan's Theorem

c. Simplification of Boolean Expressions

d. Standard Forms of Boolean Expression

e. Sum-of-Products and Product-of-Sum

f. Karnaugh Maps

V. COMBINATIONAL LOGIC

a. Implementation of combinational logic

b. Universality of NAND and NOR Gates.

c. Half & Full Adder

d. Half & Full Subtraction

e. Comparators

f. Decoders

g. Encoders

h. Multiplexers

i. Demultiplexers

VI. FLIP-FLOPS

a. Latches

b. Edge Triggered Flip-Flops

c. Operating characteristic of Flip-Flops

d. Monostable Multivibrator

e. Astable Multivibrator

VII. COUNTERS

a. Asynchronous Counters

b. Synchronous Counters

c. Up/Down Counters

d. Divide by N Counters

e. Sequential Logic Design

f. Cascaded Counters

g. Counter Applications

h. PLD Implementation of Counters

VIII. CONVERTERS

a. A/D Converters

b. D/A Converters

IV. SHIFT REGISTERS

a. Basic Shift Register operation

b. Bidirectional Shift Register

LAB SCHEDULE

Lab 1. Scope familiarization – Pulse waveforms
Lab 2. Scope familiarization – use of Delayed Sweep
Lab 3. BCD to Decimal Conversion – Inverters
Lab 4. NAND/NOR GATES
Lab 5. NAND and NOR Gate realization
Lab 6. Scope Display of LED Characteristics
Lab 7 . Simplification of Logic Equations
Lab 8 . 7-Segment LED Display]
Lab 9. Three Digit LED Display
Lab 10. Adders
Lab 11. Adders Continued
Lab 12. Flip Flops
Lab 13. Monostable/Astable Multivibrator
Lab 14. Synchronous Counter: PLD Implementation
Lab 15. Digital Clock