State University of New York Polytechnic Institute
Colleges of Nanoscale Science and Engineering

Optimization of 1.2 kV 4H-Silicon Carbide (SiC) Power Devices:
High Performance, Reliability, and Ruggedness

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ABSTRACT

Optimization of 1.2 kV 4H-Silicon Carbide (SiC) Power Devices:
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Doctor of Philosophy in Nanoscale Engineering
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This research primarily focuses on the design, fabrication, and characterization of 1.2 kV 4H-SiC devices. Power devices play a critical role in numerous high-power applications, including automotive, industrial and energy applications. The development of energy-efficient power devices is essential for reducing power loss during operation. While silicon-based power devices are widely used in high-power applications, they have reached their limit in minimizing power loss. As a result, wide-bandgap materials, particularly 4H-Silicon Carbide (SiC), have gained traction as replacements for their Silicon counterparts due to their superior material properties, enabling further reduction of power dissipation beyond Si. The demand for 1.2 kV 4H-SiC MOSFETs has significantly increased, particularly in the electric vehicle (EV) market where high performance, reliability, and ruggedness are critical to compete with Si counterparts. Hence, the optimization of 1.2 kV 4H-SiC devices is necessary.

The most distinctive feature of a power device is its ability to withstand high voltages within the drift region. The breakdown voltage of the power device is determined by the specifications of the drift region. The optimization of the drift region must be performed to enhance power efficiency for each specific application due to the trade-off relationship between on-resistance and breakdown voltage. 4H-SiC enables a thin, heavily doped drift region to
support a given breakdown voltage, resulting in a substantial reduction in the on-resistance of the device compared to Si. Moreover, Hybrid Junction Termination Extension (Hybrid-JTE) technique was employed to achieve a near-ideal breakdown voltage and experimentally verified.

The influence of deep JFET and P-well implants in 1.2 kV MOSFETs has been examined in terms of their impact on static characteristics and short-circuit ruggedness. To assess the impact on output characteristics and short-circuit ruggedness, the depths of JFET and P-well implants were compared by varying channel lengths and JFET widths. Furthermore, the significance of high channel mobility has been investigated not only for static characteristics but also for short-circuit characteristics.

The optimization of static characteristics of 1.2 kV 4H-SiC MOSFETs have been investigated through the analysis of the cell structure. A comprehensive analysis has been conducted to examine the trade-off relationship between specific on-resistance and breakdown voltage, as well as yield, by considering various dimensions within the cell structure. The dimensions explored in this analysis include the channel, JFET, contact opening, ILD (Inter-Layer Dielectric) width, and gate-to-source overlap within the cell structure.

A novel approach has been proposed to enhance the trade-off relationship between short-circuit withstand time and specific on-resistance by employing MOSFETs with a deep P-well structure through channeling implantation. For the channeling implantation, a tilt angle of 4 degrees was adjusted to <0001> direction of 4H-SiC in 4H-SiC (0001) substrates with 4 ° off-cut towered <11-20> direction. The utilization of channeling implantation has been employed to overcome the limitations associated with previous random implantation energy. The
successful fabrication and demonstration of MOSFETs with deep P-well structures using channeling implantation have been achieved.

The MOSFETs with a deep P-well structure enable the short channel lengths, which improve the trade-off relationship between specific on-resistance and breakdown voltage. The implementation of a deep P-well structure effectively suppresses the leakage current originating from the channel during the blocking-mode of operation, thereby enhancing the trade-off relationship. Additionally, the deep P-well structure has significantly reduced the maximum electric field in the gate oxide, leading to improved high temperature reverse bias (HTRB) characteristics.

A novel layout approach has been proposed and successfully demonstrated for the monolithic integration of a Schottky diode with 1.2 kV SiC MOSFETs (JBSFETs) to achieve an identical cell pitch compared to the pure MOSFET design. To further reduce cell density, highly doped JFET implantation with narrow widths of JFET/Schottky regions has been conducted. Consequently, the proposed JBSFET demonstrates comparable static performance to the pure MOSFET while exhibiting 3rd quadrant current-voltage characteristics similar to JBS diodes.

A thorough comparison of the short-circuit failure mechanisms between 1.2 kV 4H-SiC MOSFETs and Ti JBSFETs, both having identical cell pitch and specific on-resistance, has been successfully accomplished. However, despite the same channel density, different short-circuit characteristics have been observed due to the presence of leakage current from the Schottky contact in the JBSFETs. In order to comprehend the short-circuit failure mechanisms, non-isothermal mixed-mode 2D TCAD device simulations have been employed. Moreover,
based on the experimental results and analyses, potential solutions to further enhance the short-circuit characteristics of JBSFETs have been proposed.

A 1.2 kV 4H-SiC planar Junction Barrier Schottky (JBS) diode with a deep P+ grid structure, implemented through channeling implantation, has been successfully designed and fabricated. Without the use of a trench structure, a planar JBS diode with a junction depth of 2.2 μm has been successfully fabricated using an implantation energy of 350 keV. The formation of the deep junction significantly suppressed the leakage current originating from the Schottky contact.

In summary, extensive examinations have been conducted on 1.2 kV rated 4H-SiC power devices, including MOSFETs, JBSFETs, and JBS diodes, to optimize and enhance their static characteristics, dynamic characteristics, reliability, and ruggedness.
DEDICATION

To my wife, Mina Kim
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S. A. Mancini, S. Y. Jang, D. Kim, and W. Sung, "Increased 3rd Quadrant Current Handling Capability of 1.2kV 4H-SiC JBS Diode-Integrated MOSFETs (JBSFETs) with Minimal Impact on the Forward Conduction and Blocking Performances," 2021 IEEE 8th Workshop on Wide


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Chapter 1

Introduction

1.1. Advantage of 4H-SiC

Considerable attention has been focused on wide bandgap materials for future power electronic applications. In particular, 4H-Silicon Carbide (SiC) has emerged as an excellent alternative to Silicon in power electronic applications. Due to its exceptional material properties, including high electron mobility, high critical electric field, and high thermal conductivity, 4H-SiC is highly suitable for use in high-power, high-voltage, and high-temperature applications. Table 1.1 provides a comparison of the material properties of Si, 4H-SiC, GaN, β-Ga2O3, and Diamond [1]–[3].

Table 1.1. Material properties of Silicon, 4H-SiC, GaN, Ga2O3, and Diamond.

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Silicon1,2</th>
<th>4H-SiC1,2</th>
<th>GaN1,2,3</th>
<th>β-Ga2O32</th>
<th>Diamond2</th>
</tr>
</thead>
<tbody>
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<td>Energy Bandgap (eV)</td>
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<td>3.26</td>
<td>3.44</td>
<td>4.9</td>
<td>5.5</td>
</tr>
<tr>
<td>Dielectric constant (ε)</td>
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<td>9.7</td>
<td>9.5-10.4</td>
<td>10</td>
<td>5.5</td>
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<td>Electron Mobility (cm²/V·s)</td>
<td>1400</td>
<td>900</td>
<td>1200</td>
<td>300</td>
<td>~2000</td>
</tr>
<tr>
<td>Saturation velocity (cm/s)</td>
<td>1.0×10⁷</td>
<td>2.1×10⁷</td>
<td>1.4×10⁷</td>
<td>1.1×10⁷</td>
<td>2.3×10⁷</td>
</tr>
<tr>
<td>Critical Electric Field (MV/cm)</td>
<td>0.3</td>
<td>2.5</td>
<td>3.3</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm·K)</td>
<td>1.5</td>
<td>3.7</td>
<td>2.1</td>
<td>0.13-0.23</td>
<td>~10</td>
</tr>
</tbody>
</table>

One of the most significant advantages of 4H-SiC over Si, in terms of material properties for power device, is the combination of two key factors: 1) wide energy bandgap and 2) thermal conductivity. 1) The wide energy bandgap of 4H-SiC contributes to a high critical electric field and low intrinsic carrier density. The high critical field allows for the support of a designated breakdown voltage by utilizing a thin drift layer with high doping concentration, reducing the drift resistance. The low intrinsic carrier density leads to low leakage current under the blocking conditions, enabling high-temperature operation. 2) The high thermal conductivity of 4H-SiC
is crucial for its ability to withstand the degradation caused by high temperatures, making it highly suitable for applications in harsh environments. Additionally, the high thermal conductivity facilitates efficient heat dissipation from the devices, resulting in the use of smaller thermal management components.

In addition to its superior material properties, 4H-SiC offers significant advantages in device fabrication. One notable advantage is its unique characteristic of enabling relatively easy control of both n- and p-type doping over a wide doping range, distinguishing it from other wide bandgap semiconductors [4]. Furthermore, 4H-SiC has the ability to form silicon dioxide (SiO$_2$) as a native oxide, making it compatible with Silicon device structures and facilitating the integration of SiC devices with existing Silicon-based technologies [4].

Due to their high device efficiency and advantages in device fabrication, 4H-SiC power devices such as diodes based on Schottky and MOSFETs have been successfully commercialized for a wide range of applications.
Fig. 1.2. (a) Fabricated SiC MOSFETs on 6-inch SiC wafer. (b) Wafer-level characterization set-up with Cascade probe station and (c) Keithley parametric curve tracer. Test structure characterization set-up with (d) Cascade probe station and (e) Agilent B1500A. (f) Packaged devices.

Since the commercialization of SiC Schottky barrier diodes (SBDs) by Infineon and metal oxide semiconductor field effect transistors (MOSFETs) by Cree Inc (WolfSpeed) [5]–[7], extensive research has been conducted to develop power devices using SiC substrates. As a result, there has been a tremendous growth in the utilization of SiC devices across various applications, as demonstrated in Fig. 1.1 [8].

Although 4H-SiC MOSFETs have already been developed and commercialized, there is still room for further optimization of the cell structure and processes in terms of static and dynamic characteristics, reliability, and ruggedness, especially for 1.2 kV 4H-SiC devices.
1.2. Development and Optimization of 1.2 kV 4H-SiC MOSFETS

1.2 kV 4H-SiC MOSFETs, JBSFETs, and JBS diodes have been successfully fabricated at ADI and SiCamore Semi. Fig. 1.2 (a) presents the fabricated MOSFETs, JBSFETs, and JBS diodes on a 4H-SiC 6-inch wafer at ADI. The fabricated devices were evaluated through wafer-level measurements using the manual Cascade S1200 probe station and Keithley 2600 parametric curve tracer, as shown in Fig. 1.2 (b) and (c), respectively. Various parameters such as on-resistance, threshold voltage, transconductance, leakage current, breakdown voltage, and capacitance were measured. For lateral MOSFETs (FATFETs) and TLM measurements, Cascade S300 and Agilent B1500A were employed, as illustrated in Fig. 1.2 (d) and (e), respectively. The switching, short-circuit, and unclamped inductive switching were evaluated on a packaged device at Ohio State University. The fabricated devices were packaged using a TO-247 package with open cavity, as shown in Fig. 1.2 (f).

In this dissertation, the development and optimization of 1.2 kV 4H-SiC MOSFETs, JBSFETs, and JBS diodes were carried out to enhance their static and dynamic characteristics, reliability, and ruggedness. The device designs, fabrications, and characterizations of 1.2 kV 4H-SiC planar MOSFETs are thoroughly discussed. Through the optimization of the cell structure and process, a novel device structure is proposed. Chapter 2 primarily focuses on the drift design of 4H-SiC power devices. The utilization of Hybrid-JTE is employed to achieve a near-ideal breakdown voltage for the designed drift layer.

Chapter 3 describes the 1.2 kV 4H-SiC MOSFETs with different junction depths of the JFET and P-well regions. For each JFET/P-well depth combination, variations in channel lengths and JFET widths were conducted to compare specific on-resistance, breakdown voltage, and short-circuit withstand time. It was observed that a deep JFET structure provides a lower specific on-
resistance (12% lower) with a high breakdown voltage. Conversely, MOSFETs with a deep P-well exhibit a high breakdown voltage with low leakage current, even in a shorter channel length (0.4 \( \mu m \)). Moreover, the trade-off relationship between \( R_{\text{on,sp}} \) and short-circuit withstand time is discussed for MOSFETs with different JFET widths and channel lengths. The deep JFET implantation offers a better trade-off relationship due to the feasibility of narrow JFET width. To further improve this trade-off relationship, MOSFETs with deep JFET and P-well implant are proposed. Lastly, the importance of high channel mobility is investigated not only for static characteristics but also for short-circuit characteristics. The measured electrical characteristics are supported by in-depth 2D-device simulations.

Chapter 4 discusses a detailed structural analysis of 1.2 kV 4H-SiC MOSFETs with an accumulation mode channel. The experimental investigation involved fabricating and comparing various cell designs of 1.2 kV SiC MOSFETs, focusing on their output and transfer characteristics, as well as blocking behaviors. Key design parameters such as channel length, JFET width, contact openings, gate-to-source overlap, and cell pitch were thoroughly examined to quantitatively assess their impact on static performance. The experimental results were further supported by 2D simulations. The results revealed that the channel length has the most significant influence on specific on-resistance, with an increase of 0.364 m\( \Omega \)-cm\(^2\) observed per 0.1 \( \mu m \) increase in channel length. However, it was also observed that the channel potential is highly dependent on the channel length, leading to an increase in leakage current with shorter channel designs. The incorporation of enhanced doping in the JFET region with a current spreading layer (CSL) proved crucial in achieving a narrower JFET width, thereby satisfying the requirements for static performance, device reliability, and ruggedness. Additionally, this paper explores potential methods to further enhance the trade-off characteristics through other design aspects.
In Chapter 5, non-isothermal simulations were conducted to understand the short-circuit (SC) behavior of SiC MOSFETs. Using the established model, structures were proposed to enhance the SC ruggedness. It was found that a thin gate oxide and a narrow JFET region can reduce saturation current and improve SC ruggedness without increasing $R_{on,sp}$. The results indicate that a thin gate oxide offers moderate improvement in SC capability but comes at the cost of increased $C_{gs}$. On the other hand, a narrow JFET region provides much-improved (2×) SC ruggedness, as well as lower $R_{on,sp}$, without negatively impacting $C_{gs}$.

Chapter 6 describes the layout approaches and resulting static, dynamic, and short-circuit (SC) ruggedness characteristics of 1.2 kV power MOSFETs fabricated on a 6-inch 4H-SiC substrate. Different layout topologies, including linear and hexagonal, as well as various design variations with and without a bridge of P-well, were investigated to understand their effect. The experimental results demonstrated the following findings: 1) the hexagonal layout topology enables a low specific on-resistance ($R_{on,sp}$), 2) the linear MOSFET exhibits fast switching speed and is suitable for high-frequency applications, and 3) the hexagonal topology with a bridge offers greater reliability and ruggedness.

Chapter 7 introduces and demonstrates the operation of 1.2 kV 4H-SiC MOSFETs with a low knee voltage and forward voltage drop in the third quadrant mode, aimed at eliminating the need for external SiC SBDs in power converter applications. The proposed MOSFETs utilize optimized accumulation mode channels and a simplified fabrication process that eliminates the epitaxial regrowth step. Various channel design parameters, including doping concentration, channel length, and gate oxides, were investigated to achieve low knee voltage and forward voltage drop under third quadrant operation while ensuring high breakdown voltages under blocking operation. The impact of channel potential (barrier) on current conduction behavior and leakage current during
third quadrant operation and the blocking mode, respectively, was studied through 2D simulations. Furthermore, the reverse recovery characteristics and switching behavior of the devices are discussed. The optimized channel design serves as a significant breakthrough in the development of highly promising devices for high-density power electronics applications.

In Chapter 8, a novel device structure was introduced to significantly enhance the trade-off relationship between specific on-resistance and short-circuit withstand time in 1.2 kV 4H-SiC MOSFETs. MOSFETs with deep P-wells formed using channeling implantation were firstly demonstrated to enhance short-circuit ruggedness, achieving approximately four times longer withstand time compared to conventional MOSFETs. This enhancement was achieved without any negative impact on specific on-resistance, resulting in MOSFETs with a short-circuit withstand time of 8 μs. To form deep P-well junctions, a channeling implantation technique with low energy was employed. Importantly, the fabrication process for the deep P-well using channeling implantation was demonstrated to be straightforward and did not require additional or complicated steps when compared to the conventional MOSFET fabrication process. A comprehensive comparison between the conventional and novel designs was conducted, considering the output characteristics, blocking behaviors, and short-circuit ruggedness.

Chapter 9 introduces 1.2 kV 4H-SiC MOSFETs with a deep P-well structure achieved through channeling implantation to enable a short channel length. The utilization of channeling implantation allowed for the formation of deep junctions with low energy implantation. The proposed MOSFETs, with a short channel of 0.3 μm, demonstrated low leakage current and high breakdown voltage, contrasting with conventional MOSFETs of similar ratings exhibited significant leakage current. The incorporation of a deep P-well structure effectively suppressed the leakage current from the channel during the forward blocking mode. Consequently, the specific
on-resistance of the proposed MOSFETs with a channel length of 0.3 μm was reduced by approximately 10%. Furthermore, the conventional trade-off relationship between specific on-resistance and short-circuit withstand time was improved in the proposed MOSFETs due to the presence of the deep P-well structure. Experimental measurements of output, blocking, and short-circuit characteristics were conducted on fabricated 1.2 kV SiC MOSFETs, supported and clarified by the use of Sentaurus 2D TCAD.

Chapter 10 presents the development and evaluation of a 1.2 kV 4H-SiC Split-Gate (SG) MOSFET with a deep P-well structure, which effectively reduces the maximum electric field in the gate oxide (E_{OX}), increases the short-circuit withstand time (SCWT), and reduces the switching energy loss. Channeling implantation was employed to achieve a deep junction with low implantation energy in the proposed SG-MOSFET. The conventional MOSFET, conventional SG-MOSFET, and proposed SG-MOSFET were successfully fabricated and evaluated. A comparison of the measured static, dynamic, and short-circuit characteristics was conducted. Furthermore, 2D simulations were performed to validate the experimental results and analyze the electric field in the gate oxide. The proposed SG-MOSFET outperforms the conventional SG-MOSFET with a 1.06× increase in breakdown voltage (BV) and a 1.78× decrease in E_{ox}. Additionally, the proposed SG-MOSFET exhibits a 1.52× improvement in SCWT compared to the conventional SG-MOSFET. Further, the proposed SG-MOSFET enhances \( R_{on} \times C_{rss} \) by 2.66× compared to the conventional SG-MOSFET, leading to a 1.5× reduction in E_{off} and a 1.05× reduction in E_{total}.

Chapter 11 proposes the demonstration of 1.2 kV 4H-SiC Schottky-integrated MOSFETs (JBSFETs) that achieve the same specific on-resistance as the pure MOSFETs by utilizing an innovative layout approach and a novel deep P-well structure. The proposed JBSFETs significantly reduce the specific on-resistance, resulting in a 2× reduction in the chip size compared to the
traditional chip-to-chip parallel connection of separate MOSFETs and JBS diodes. Additionally, the leakage current originating from the Schottky contact is effectively suppressed by implementing a 1.8 µm deep P-well structure through channeling implantation. This paper discusses the device design strategy, layout approach, fabrication process, and static and short-circuit characteristics of the proposed JBSFETs. Furthermore, 2D simulations are conducted to further comprehend and elucidate the experimental results.

Chapter 12 compares 1.2 kV 4H-SiC MOSFETs and Ti JBSFETs with deep P-well structures. To ensure a fair comparison of their short-circuit characteristics, an innovative design approach was applied to the JBSFETs to achieve the same specific on-resistance as the MOSFETs. To enhance the short-circuit characteristics of both the MOSFETs and JBSFETs, channeling implantation was conducted to form a deep P-well structure, which helps reduce the maximum saturation current during the short-circuit events. This approach resulted in improved short-circuit characteristics in both device types. However, the JBSFETs exhibited a shorter short-circuit withstand time compared to the MOSFETs due to the high leakage current from Schottky contact. Sentaurus 2D TCAD simulations were utilized to gain a deeper understanding of the short-circuit mechanisms in the MOSFETs and JBSFETs. It was observed that the MOSFETs failed due to the high current in the channel region, while the failure of JBSFETs occurred at the Schottky contact. Furthermore, potential solutions to enhance the short-circuit characteristics of JBSFETs were proposed, including the adoption of a narrower Schottky width and a high work function metal.

Chapter 13 presents a study on enhancing the reverse characteristics of 1.2 kV 4H-SiC JBS diodes by incorporating a deep P+ grid structure. To achieve a deep junction with low implantation energy, channeling implantation was utilized. Diodes with different junction depths of the P+ grid were fabricated to compare their forward and reverse I-V characteristics, specifically at depth of
0.8 μm, 1.4 μm, and 2.2 μm. Regardless of the P+ grid depth, nearly identical forward I-V characteristics were obtained. However, the deeper P+ grid junction significantly suppressed the leakage current, resulting in leakage current values of 60 μA, 1.5 μA, and 1.7 nA (at 1200 V) for the 0.8 μm, 1.4 μm, and 2.2 μm P+ grid junctions, respectively. Despite the implementation of a deep junction using channeling implantation, the proposed JBS diode achieved high breakdown voltages comparable to those of shallow junction diodes. This can be attributed to the relatively low doping concentration in the deep junction. Furthermore, different edge termination structures with various main junction depths were discussed. To achieve a near-ideal breakdown voltage unaffected by the JTE (Junction Termination Extension) dose, Hybrid-JTE was employed. The study demonstrated that the proposed JBS diodes attained high breakdown voltages and significantly reduced leakage current using the same edge termination technology as conventional shallow junction diodes. To gain a better understanding of the impact of the deep junction, 2D simulations were conducted.

Chapter 14 provides a comprehensive summary of the significant accomplishments of this work, as well as discussing future work.

1.3. REFERENCES


Chapter 2

Design of 1.2 kV Planar SiC MOSFETs

2.1. Drift Layer Design for 1.2 kV 4H-SiC Power MOSFETs

The most notable characteristic of a power device is its ability to withstand high voltages. During the blocking mode of operation, the drift layer plays a crucial role in supporting the voltages, and the breakdown voltages of the power device depend on the thickness and doping concentration of the drift layer. Therefore, optimizing the drift layer is imperative in achieving low specific on-resistance and high breakdown voltages for power devices.

Due to the high critical electric field exhibited by 4H-SiC, thinner thicknesses and higher doping concentrations can be employed in its drift layer to achieve the desired breakdown voltages compared to what is achievable with a Si drift layer. This, in turn, leads to significantly lower drift resistance in 4H-SiC drift layers.

In power device drift layer design, two approaches are commonly used: Punch-Through (PT) and Nonpunch-Through (NPT) designs. Fig. 2.1 (a) and (b) illustrate the electric field distribution in a PiN diode under PT and NPT designs. The PT design achieves the same breakdown voltage as the NPT design by utilizing a thinner drift layer and lower doping concentration. The electric field takes on a trapezoidal shape for the PT design and a triangular shape for the NPT design, as shown in Fig. 2.1 (c). Due to the favorable electric field shape of the PT design, it offers a 14.9% lower specific on-resistance than the NPT design in unipolar devices [1].

In this dissertation, the PN design concept was implemented on a 4H-SiC epitaxial layer to develop a power device with a low specific on-resistance and a breakdown voltage rating of 1200
Fig. 2.1. Schematic of the parallel plane for (a) punch-through and (b) nonpunch-through drift layer design. (c) The electric field distribution of both designs.

V. However, considering edge termination efficiency and voltage overshoot, a targeted breakdown voltage of 1700 V was set as the ideal case. For the 1700 V power device, a 4H-SiC drift thickness of 10 μm and a drift doping concentration of $8 \times 10^{15}$ cm$^{-3}$ were employed.

2.2. AVALANCHE BREAKDOWN

The blocking characteristics of power devices are determined by the avalanche breakdown phenomenon, where carriers gain enough energy from a high electric field to create electron-hole pairs upon colliding with lattice atoms. This impact ionization process governs the current flowing through the depletion region when subjected to a significant electric field. The impact ionization
Fig. 2.2. Impact ionization coefficient for holes as a function of the inverse of the electric field.

Fig. 2.3. Impact ionization coefficient for electrons as a function of the inverse of the electric field.

coefficient represents the number of electron-hole pairs created by a mobile carrier traversing 1 cm through the depletion region in the direction of the electric field. The impact ionization coefficients for electrons and holes exhibit a strong dependence on the electric field magnitude, as illustrated in Fig. 2.2 and Fig. 2.3. In 4H-SiC, the impact ionization coefficient for holes is notably
higher than that of electrons, indicating that the ionization integral of holes generally reaches unity earlier than that of electrons with increasing electric field strength [2], [3]. In the simulation, the breakdown voltage was determined by utilizing the ionization integral for holes initiated by impact ionization (phihole).

Fig. 2.2 and Fig. 2.3 show the impact ionization coefficients for holes and electrons as a function of the inverse of the electric field, incorporating various models reported by different research groups [4]–[6]. The coefficients for electrons were slightly adjusted based on the Konstantinov model to achieve better alignment between the model and experimental results. The equations representing the adjusted coefficients are as follows:

\[ \alpha = 2.59 \times 10^6 \exp \left( -\left( \frac{9.19 \times 10^6}{E} \right)^{1.6} \right) [cm^{-1}] \quad (eq. 1) \]

\[ \beta = 3.32 \times 10^6 \exp \left( -\left( \frac{1.07 \times 10^7}{E} \right)^{1.1} \right) [cm^{-1}] \quad (eq. 2) \]

The condition for avalanche breakdown in a diode occurs when the impact ionization rate reaches infinity. The total number of electron-hole pairs generated in the depletion region, resulting from a single electron-hole pair that was initially created a distance x away from the junction, is mathematically expressed by equations derived by:

\[ M(x) = 1 + \int_0^x \alpha_n M(x) dx + \int_x^W \alpha_p M(x) dx \quad (eq. 3) \]

where W is the width of the depletion region. A solution for this equation is given by:

\[ M(x) = M(0) \exp \left( \int_0^x (\alpha_n - \alpha_p) dx \right) \quad (eq. 4) \]

where M(0) is the total number of electron-hole pairs at the edge of the depletion region. Using eq. 3 with x=0 provides a solution for M(0):
\[
M(0) = \left\{ 1 - \int_0^W \alpha_p \exp \left[ \int_0^x (\alpha_n - \alpha_p) \, dx \right] \, dx \right\}^{-1} \quad (eq. 5)
\]

Using this expression in Eq. 4 gives:

\[
M(x) = \frac{\exp[\int_0^x (\alpha_n - \alpha_p) \, dx]}{1 - \int_0^W \alpha_p \exp[\int_0^x (\alpha_n - \alpha_p) \, dx] \, dx} \quad (eq. 6)
\]

The multiplication coefficient, \( M(x) \), represents the total number of electron-hole pairs created in response to the generation of a single electron-hole pair at a distance \( x \) from the junction, provided that the electric field distribution along the impact ionization path is known. The avalanche breakdown condition is defined as the point where the total number of electron-hole pairs generated within the depletion region approaches infinity, which corresponds to the multiplication coefficient \( M \) becoming infinite. The condition of infinite multiplication coefficient (\( M \)) that defines the avalanche breakdown is achieved by equating the denominator of Eq. 6 to zero:

\[
\left\{ \int_0^W \alpha_p \exp \left[ \int_0^x (\alpha_n - \alpha_p) \, dx \right] \, dx \right\} = 1 \quad (eq. 7)
\]

The left-hand side of Eq. 7 is commonly referred to as the ionization integral and is used in the analysis of avalanche breakdown in power devices. It is a common practice to determine the voltage at which the ionization integral equals unity. Assuming that the impact ionization coefficients for electrons and holes are equal, the avalanche breakdown condition can be expressed as:

\[
\int_0^W \alpha \, dx = 1 \quad (eq. 8)
\]
2.3. EDGE TERMINATION

The edge termination structures are required for the power devices. The finite area of a power device leads to cylindrical or spherical junctions at its edges, which in turn result in high electric fields. This high electric field causes a reduction in the breakdown voltage of the device. Therefore, edge termination structures are necessary for power devices to minimize the reduction in the breakdown voltage from the edge of the device. A superior edge termination is particularly crucial for 4H-SiC power devices to fully exploit their superior material properties for blocking characteristics, such as low leakage current resulting from the low intrinsic carrier density and high breakdown voltage due to the high critical electric field.

Various edge termination techniques have been proposed and demonstrated in 4H-SiC power devices, including but not limited to field plate termination, resistive termination, bevel termination, floating field rings (FFRs), and junction termination extension (JTE) [7]–[20]. Out of the various edge termination methodologies, FFRs and JTE have been utilized as the most widely employed techniques in 4H-SiC power devices. However, the sensitivity of FFRs to the fabrication process, which requires precise critical dimensions and a stable angle of the hard mask to maintain high breakdown voltages, makes it difficult to use them as an edge termination structure.

A wide range of JTE structures has been reported, including single-zone (SZ)-JTE, multi-zone-JTE, etched/mesa-JTE, space-modulated-JTE, and other modified forms [11]–[17]. When using JTE-based terminations, achieving a specified breakdown voltage is heavily dependent on the implanted dose, making it critical to target an optimum charge in the JTE region. To improve the process window, multi-zone and etched/mesa JTE structures have been introduced since SZ-JTE is highly sensitive to impurity dose. However, the multi-zone approach necessitates additional masking steps, which can make the process more complicated, while the etched/mesa JTE and
related structures require precise control of the etching process to modulate the JTE charge. Aiming to address the sensitivity of JTE-based terminations to impurity dose and process variability, Ring Assisted (RA-), Multiple Floating Zone (MFZ-), and Hybrid-JTEs have emerged as promising edge termination structures [18]–[20].

In this chapter, SZ-, RA-, MFZ-, and Hybrid-JTE structures for 1200 V-rated will be investigated and discussed, with a wide range of implantation doses.

### 2.3.1. Single Zone – Junction Termination Extension (SZ-JTE)

Fig. 2.4 shows the cross-sectional view of PiN diodes without edge termination and with SZ-JTE. Without edge termination structure was utilized as a reference to demonstrate the critical role of edge termination structures. In the SZ-JTE structure, a lightly doped P-type region, referred to
as a junction-termination-extension (JTE), is placed adjacent to the P+ main junction. The primary objective of implementing the SZ-JTE structure is to reduce the electric field crowding at the P+ junction by creating an additional electric peak at the end of the SZ-JTE region, thereby enhancing breakdown voltages, as depicted in Fig. 2.5.
The simulated electric field as a function of distance is presented in Fig. 2.6. The device without an edge termination structure exhibits an abrupt electric field peak at the end of the P+ main junction, which leads to a low breakdown voltage of 515 V. However, the SZ-JTE structure helps to mitigate electric field crowding at the P+ main junction by creating an additional electric field peak at the end of the SZ-JTE region, which contributes to an improvement in the breakdown voltage.

The performance of the SZ-JTE is highly influenced by the width and implant dose of the JTE (P-) region. The width of the JTE region should be at least 3 to 5 times the thickness of the drift layer to ensure a high breakdown voltage with consistent device yield [17]. The breakdown voltage of the device is determined by the dose of JTE, as demonstrated in Fig. 2.5. It is discovered that the SZ-JTE is extremely sensitive to the dose for achieving high breakdown voltages. When the JTE dose is lower than the optimum dose, the SZ-JTE cannot effectively alleviate the electric field at the main junction, resulting in the highest electric field occurring at the P+ main junction, as shown in Fig. 2.7. On the other hand, a higher JTE dose compared to the optimum dose results in
Fig. 2.8. A schematic cross-sectional view of PiN diodes with RA-JTE structure.

a lower breakdown voltage since the highest electric field occurs at the edge of the JTE region, similar to the case without an edge termination structure, as shown in Fig. 2.7. During the fabrication process, incomplete activation of Aluminum and fixed charges of oxide can affect the effective JTE dose, making it difficult to achieve the targeted JTE dose accurately. Due to the sensitivity of the SZ-JTE structure and process variation, it is challenging to use it as an effective edge termination structure.

2.3.2. RING ASSISTED – JUNCTION TERMINATION EXTENSION (RA-JTE)

In order to resolve the sensitivity to dose, Ring Assisted (RA) – JTE has been introduced [18]. Fig. 2.8 shows the schematic cross-sectional view of the RA-JTE structure. The insertion of a P+ floating ring in the SZ-JTE structure can effectively reduce the electric field at the P+ main junction, particularly for lower JTE doses in comparison to the optimum dose. This approach widens the process window and provides a direct solution to the issues associated with the sensitivity of the SZ-JTE structure.

To fully utilize the benefits of P+ floating rings in the SZ-JTE, the design of the RA-JTE structure should be optimized for the initial spacing between the first floating ring and the main junction ($S_0$), as well as the incremental spacing between subsequent floating rings ($S_i$). The
Fig. 2.9. A simulated breakdown voltage of SZ-JTE and RA-JTE as a function of JTE dose.

Fig. 2.10. Simulated electric field distribution of RA-JTE structure at low JTE dose.
placement of the RA-JTE is defined by the equation:

\[ S_n = S_0 + S_i(n - 1) \]

, where \( S_n \) is the corresponding spacing with respect to the number of rings, \( S_0 \) is the initial spacing of the ring from the main P+ junction, \( S_i \) is the incremental spacing of the ring, and \( n \) is the number of rings.

Based on the simulated results, the RA-JTE structure for 1.2 kV rating was optimized with \( S_0 \) of 4 μm, \( S_i \) of 1 μm, and \( n \) of 3. Fig. 2.9 shows the simulated breakdown voltage of SZ-JTE and optimized RA-JTE as a function of the JTE dose. RA-JTE provides a wider process window to achieve high breakdown voltage compared to SZ-JTE by utilizing P+ floating rings in the JTE structure. The P+ floating rings distribute the electric field of the main P+ junction in low JTE dose, as shown in Fig. 2.10, enabling the device to achieve a high breakdown voltage with reduced sensitivity to JTE dose.

2.3.3. **Multiple Floating Zone – Junction Termination Extension (MFZ-JTE)**

The RA-JTE structure has been shown to widen the process window for lower JTE doses. To further increase the process window for higher JTE doses compared to the optimum dose of the SZ-JTE structure, the Multiple Floating Zone (MFZ) – JTE has been introduced [18], [19]. Fig. 2.11 depicts a schematic cross-sectional view of the MFZ-JTE structure, which is designed to implement a gradual distribution of the JTE dose. The dose in the JTE region is reduced through the use of variable masking that gradually increases in dimension towards the JTE edge. This approach achieves a similar effect as multiple consecutive JTE zones while only requiring a single implant process. Each zone in the MFZ-JTE structure has an identical dose but is separated by a
Fig. 2.11. A schematic cross-sectional view of PiN diodes with MFZ-JTE structure.

Fig. 2.12. A simulated breakdown voltage of SZ-JTE and MFZ-JTE as a function of JTE dose.

different space that increases from the main junction towards the edge of the termination structure. This arrangement results in a gradual decrease in average charges in the JTE regions, as the width of each zone is gradually decreased by the ratio of "β". Proper selection of β and the number of zones (n) enables the implementation of MFZ-JTE for achieving a high breakdown voltage with a wider process window, without the need for additional implant processes. Based on the simulated results, the MFZ-JTE structure for a 1.2 kV rating was optimized with a β of 1.05 and n of 12.
Fig. 2.12 shows the simulated breakdown voltage of SZ-JTE and MFZ-JTE as a function of the JTE dose. When the JTE dose is below the optimum dose, the MFZ-JTE structure exhibits blocking characteristics similar to those of the SZ-JTE structure. This is due to the insufficient charge in the MFZ-JTE to mitigate the high electric field at the P+ main junction, which is similar to the SZ-JTE structure. On the other hand, when the JTE dose exceeds the optimum dose, the MFZ-JTE structure achieves high breakdown voltages by distributing the electric field at each zone, as shown in Fig. 2.13, thereby reducing the electric field at the edge of the JTE region. It is demonstrated that the gradual charge distribution of the JTE zones allows for a high breakdown voltage at higher JTE doses, resulting in an increased process window.
2.3.4. Hybrid – Junction Termination Extension (Hybrid-JTE)

Through investigation and analysis, it has been determined that the implementation of the RA-JTE structure facilitates achieving high breakdown conditions at lower JTE doses, whereas the utilization of the MFZ-JTE structure widens the process window at higher JTE doses. Following the aforementioned optimizations of both the RA-JTE and MFZ-JTE structures, the establishment of a Hybrid-JTE can be achieved by combining the RA-JTE and MFZ-JTE, as detailed in references [18], [20]. Fig. 2.14 shows a schematic cross-sectional view of the Hybrid-JTE structure.

One of the primary issues concerning the edge termination of 4H-SiC devices based on JTE is their sensitivity to JTE charge. Achieving the targeted JTE charge is challenging in 4H-SiC, primarily due to the incomplete activation of Aluminum and the impact of fixed charges, which results in considerable variations in the charge. However, the Hybrid-JTE approach overcomes this challenge by allowing a wide range of JTE doses to achieve high breakdown voltage through the superposition of RA-JTE and MFZ-JTE. At low doses, RA-JTE plays a crucial role in achieving high breakdown voltage, while at high doses, MFZ-JTE widens the process window.

![Hybrid-JTE structure](image)

Fig. 2.14. A schematic cross-sectional view of Hybrid-JTE structure.
Fig. 2.15. A simulated breakdown voltage of SZ-JTE, RA-JTE, MFZ-JTE, and Hybrid-JTE as a function of JTE dose.

Fig. 2.16. Simulated electric field distribution of Hybrid-JTE at lower JTE dose and higher JTE dose when compared to the optimum dose.
Fig. 2.15 shows the breakdown voltage as a function of the JTE dose of SZ-JTE, RA-JTE, MFZ-JTE, and Hybrid-JTE. The Hybrid-JTE structure provides a significantly wider process window, effectively addressing the sensitivity to JTE dose observed in JTE-based edge termination. A simulated electric field distribution for Hybrid-JTE with different JTE doses is shown in Fig. 2.16. It is evident that RA-JTE plays a significant role in supporting most of the electric field at low doses, while MFZ-JTE demonstrates an improved ability to manage the electric field distribution at high doses.

In conclusion, the Hybrid-JTE approach allows for fabrication with a wide process window of JTE dose, without significant concern for variations in JTE dose, ensuring high-performance device fabrication.

2.4. CHALLENGE OF 1.2 kV 4H-SiC MOSFETS

Despite optimization and development efforts since the commercialization of SiC MOSFETs, they still face several challenges such as cost, channel mobility, bias-induced threshold voltage Instability (BTI), high temperature reverse bias (HTRB), body diode degradation, and short-circuit characteristics.

2.4.1. Cost

The cost of 1.2 kV 4H-SiC MOSFETs is approximately three times higher than that of 1.2 kV Si IGBTs [21], [22]. Despite the potential benefits of using SiC MOSFETs to reduce system cost, weight, and volume, the high chip cost remains a significant barrier to replacing Si counterparts. There are several factors that contribute to the high cost of SiC MOSFETs. First, the cost of SiC wafers is higher than that of Si due to the significantly higher growth temperatures required and
Fig. 2.17. (a) The effect of specific on-resistance on the active area. (b) The chip size and chip size reduction as a function of the current rating, depending on edge termination widths. (c) The impact of thermal resistance on the active size.
the smaller diameter of the wafer size [23], [24]. Furthermore, the manufacturing process for SiC devices is more expensive due to the need for higher temperature processes and higher energy implantation compared to Si devices.

Various strategies still exist to reduce the cost of 4H-SiC power devices, including large-scale production on 4H-SiC wafers, optimizing the active area and edge termination structure to reduce chip size, developing advanced packaging schemes such as double-sided cooling to reduce the thermal resistance, and conducting most implantations at room temperature, except for P+ body implantation [25]–[27]. Moreover, channeling implantation can be used to form a deep junction using low energy implantation [28], [29].

Fig. 2.17 (a) illustrates the effect of specific on-resistance on the active area. The formulation for calculating the active area is as follows:

\[ A = \sqrt{\frac{I^2 \times k \times R_{on,sp,300K} \times \left(\frac{T_{j,max}}{300}\right)^\alpha}{T_{j,max} - T_c}} \text{[cm}^2]\] [25]

where A denotes the active area, k represents the thermal resistance, \( T_{j,max} \) is the maximum junction temperature, \( T_c \) is the case temperature, \( \alpha \) is the temperature coefficient, and \( R_{on,sp,300K} \) is the specific on-resistance at room temperature (RT). The thermal resistance value of 0.068 [Kcm\(^2\)/W] was adopted from [25]. It can be expected that the active area is proportional to the square root of the specific on-resistance. In Fig. 2.17 (a), the reduction in active area was calculated by comparing \( R_{on,sp} \) of 2.0 mohm-cm\(^2\). Achieving a 2.5 times lower specific on-resistance resulted in approximately a 37\% reduction in the active area. These significant improvements can be attained by enhancing the channel mobility and increasing the cell density.

Fig. 2.17 (b) shows the the chip size and chip size reduction as a function of the current rating, depending on edge termination widths. The total chip size encompasses the summation of the
active area, periphery area, edge termination, and dicing line. The reduction in the chip size was calculated by comparing the edge termination of 60 μm. Lower current rating devices notably affected by the width of edge termination structures. Specifically, at a current of 20 A, the chip size was reduced by 10.4% and 5.4% when the edge termination width was decreased from 180 μm to 60 μm and from 120 μm to 60 μm, respectively. The reduction in edge termination width can be achieved by utilizing RA-JTE instead of Hybrid-JTE, once the JTE structure is optimized.

The impact of thermal resistance on the active size is depicted in Fig. 2.17 (c), considering a device with a specific on-resistance of 3.5 mohm-cm². As mentioned earlier, advancements in packaging technology, such as double-sided cooling or flip-chip techniques [25], can help reduce thermal resistance and subsequently decrease the active size of the devices. However, it is important to take into account the additional cost associated with implementing advanced packaging technologies.

2.4.2. CHANNEL MOBILITY

4H-SiC allows for a much thinner and higher doped drift layer, capable of supporting a given breakdown voltage when compared to Si. 4H-SiC MOSFETs have been extensively researched and developed as a potential replacement for Si IGBTs due to their superior material properties. Despite the lower drift resistance of 4H-SiC, achieving a significant reduction in the specific on-resistance of 1.2 kV 4H-SiC MOSFETs has been challenging due to the low channel mobility. The critical issue of the gate oxide has been reported regarding the high interface state density (D_{it}) and rough surface, which dramatically reduces channel mobility.

Channel mobility is limited by surface phonon scattering, Coulomb scattering, and surface roughness scattering. Moreover, electrons in the channel are subject to the same scattering
mechanisms as those in the bulk. The total channel mobility is assumed to result from Matthiessen’s rule [30], [31]:

\[
\frac{1}{\mu_{CH}} = \frac{1}{\mu_B} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}}
\]

where \(\mu_B\) is the bulk mobility, \(\mu_{PH}\) is the mobility due to surface phonon scattering, \(\mu_C\) is the mobility due to Coulomb scattering, and \(\mu_{SR}\) is the mobility due to surface roughness scattering.

The channel mobility of 4H-SiC MOSFETs is significantly influenced by Coulomb scattering and surface roughness. During typical operating conditions, particularly at low gate voltages, the channel mobility in SiC MOSFETs is primarily affected by Coulomb scattering caused by interface traps and fixed oxide charges [32], [33]. At low gate voltages, the inversion charge in SiC MOSFETs is significantly lower, but the number of occupied traps is relatively high. This leads to a small screening effect and a substantial Coulomb scattering of mobile charges by occupied traps and fixed charges, causing a dominant degradation mechanism of channel mobility. On the other hand, when the gate voltage is high, the inversion charge in SiC MOSFETs is significantly higher, resulting in an effective screening effect on the occupied traps and the fixed charge. This results in a decrease in the impact of Coulomb scattering and an increase in the influence of surface roughness on the degradation mechanism of channel mobility.

Dry oxidation of 4H-SiC MOSFETs has been shown to result in a high interface trap density, leading to a peak channel mobility of approximately 2 cm\(^2\)/Vs [34]. Post oxidation annealing (POA) in nitric oxide (NO) or nitrous oxide (N\(_2\)O) has been shown to significantly reduce the interface trap density, resulting in a high channel mobility of approximately 30 cm\(^2\)/Vs [34], [35]. Several research groups have reported a peak channel mobility exceeding 100 cm\(^2\)/Vs at low gate voltages using various gate oxide types, including Phosphorus-doped gate oxide, Al\(_2\)O\(_3\), and Lanthanum Silicate with atomic layer deposited SiO\(_2\) [36]–[38]. However, mobility starts to
decrease rapidly with increasing gate voltages. Among these methods, post oxidation annealing (POA) in nitric oxide (NO) has become a standard process in SiC MOSFETs due to its effectiveness in reducing interface trap density while maintaining gate oxide reliability [35].

Another important factor in increasing channel mobility is the reduction of the effective normal field to enhance mobility caused by surface roughness. Surface roughness scattering is inversely proportional to the square of the effective surface field:

\[ \mu_{SR} \propto E_{eff}^{-2} \]

\[ E_{eff} = \frac{1}{\varepsilon_s} \left( \frac{Q_N}{2} + Q_D \right) \]

where \( E_{eff} \) is the effective normal field, \( Q_N \) is the sheet charge density, and \( Q_D \) is the charge per unit area in the depletion region.

\[ Q_D = -C_{ox} \sqrt{2V_0(2\psi_F + V_R)} \]

where \( \psi_F \) is the bulk potential. The higher bandgap energy and lower dielectric constant of 4H-SiC compared to Si result in a higher effective normal field, which leads to more degradation caused by surface roughness in 4H-SiC. The lower channel doping concentration was designed to reduce the effective normal field, and thus higher channel mobility was achieved compared to a higher channel doping concentration [39], [40]. To further enhance channel mobility, MOSFETs with the accumulation mode channel (n-type channel) have been proposed and developed [41], [42]. The wide bandgap material of 4H-SiC creates a large built-in potential, making it possible to utilize an n-type channel for nMOSFETs, which are typically designed as normally-off devices. Utilizing an accumulation mode channel in 4H-SiC MOSFETs has two crucial benefits for improving channel mobility. Firstly, it reduces the effective normal field, which can increase mobility for surface roughness. Secondly, nitrogen implantation to create the accumulation mode
Fig. 2.18. A schematic cross-sectional view of FATFET structure: (a) accumulation mode channel and (b) inversion mode channel.

Fig. 2.19. (a) The ideal universal curve, calculated based on the formulated values of $\mu_{\text{phonon}}$ and $\mu_{\text{SR}}$, using Matthiessen’s rule [30]. (b) The measured transfer characteristics and extracted channel mobility of FATFETs with accumulation mode channel and inversion mode channel.

channel can reduce interface traps, resulting in improved mobility caused by Coulomb scattering [43], [44].

Fig. 2.18 shows a schematic cross-sectional view of the FATFET structure, which is a lateral MOSFET with long channel lengths: (a) accumulation mode channel and (b) inversion mode channel. Both the accumulation and inversion mode channels use thermal gate oxide with NO POA.
The ideal $\mu_{\text{Hall}}$ is crucial when Coulomb scattering is not the dominant factor. Fig. 2.19 (a) shows the ideal universal curve, calculated by considering the formulated values of $\mu_{\text{phonon}}$ and $\mu_{\text{SR}}$, utilizing Matthiessen’s rule [30]. The formulations for $\mu_{\text{phonon}}$ and $\mu_{\text{SR}}$ are as follows:

$$\mu_{\text{phonon}} \propto 66.5 \times E_{\text{eff}}^{-0.39} [30]$$
$$\mu_{\text{SR}} \propto 76.7 \times E_{\text{eff}}^{-2} [30]$$

Despite utilizing the accumulation mode channel with NO POA, the maximum channel mobility remains limited to approximately 25 cm$^2$/Vs, resulting in high channel resistance, as shown in Fig. 2.19 (b). Unlike the ideal universal curve, the experimental results exhibited low channel mobility attributed to high interface trap. Due to the significant impact of channel mobility on the on-resistance of 1.2 kV 4H-SiC MOSFETs, shorter channel lengths are required to minimize the effect of low channel mobility [45], [46].

### 2.4.3. Bias-Induced Threshold Voltage Instability (BTI)

In high-power applications, devices are often connected in parallel to increase the maximum current. The parallelization efficiency is influenced by the matching of the on-resistance and threshold voltage of each device. The non-uniform degradation of the threshold voltage caused by bias-induced threshold voltage Instability (BTI) can result in uneven current distributions within the system, leading to degraded commutation efficiency and increased module temperature [47]–[49].

A positive shift of the threshold voltage can lead to a reduction in the overdrive of the on-state, resulting in an increase in the channel resistance of individual devices. This degradation in efficiency can result in an increase in static losses and module temperature. During fast switching,
parasitic turn-on may occur due to a gradual negative drift of the threshold voltage caused by BTI, causing the device to have a threshold voltage below a critical value [47].

BTI is predominantly caused by the presence of interface trapped charges such as dangling bond-like or vacancy-like centers and border traps including oxygen vacancies, interstitials, carbon-dimers, hydroxyl E’ centers, or silicon-oxygen bonds with wide O-Si-O angles and elongated bond length [47]. The poor BTI characteristics of 4H-SiC MOSFETs can be attributed to the inferior quality of the gate oxide caused by high interface trapped charge and border traps, combined with the narrower band offsets due to the wide band gap of 4H-SiC, which increases the tunneling probability [47]–[49].

Fig. 2.20 shows the threshold voltage shifts for positive bias-stress and negative bias-stress of the fabricated MOSFETs with different gate oxides and POA conditions. Due to the better quality of thermal oxidation, thermal gate oxide provides lower $V_{th}$ shifts regardless of POA conditions. To minimize the threshold voltage shift caused by BTI in 4H-SiC MOSFETs, thermal oxidation is required.
2.4.4. High Temperature Reverse Bias (HTRB)

During high temperature reverse bias (HTRB) test, the failure of 4H-SiC MOSFETs occurs in the middle of the JFET region. The device failure is due to the sudden rise in the gate leakage current rather than an increase in the drain leakage current. After undergoing stress testing, failed devices exhibit a faulty or shorted gate oxide, although they still possess low leakage while blocking voltage [50]–[52]. 4H-SiC MOSFETs exhibit a high surface electric field (>1 MV/cm) in the JFET region. Moreover, the low dielectric constant of the gate oxide further increases the electric field in the gate oxide. As a result, the gate oxide breakdown occurs under HTRB testing, leading to device failure.

![Electric Field Distribution](image)

Fig. 2.21. A simulated electric field distribution of 4H-SiC MOSFETs at a drain voltage of 1200 V.

Fig. 2.21 shows a simulated electric field distribution of 4H-SiC MOSFETs at a drain voltage of 1200 V. As mentioned earlier, the maximum electric field occurs at the gate oxide in the middle of the JFET region. To mitigate the maximum electric field in the gate oxide and improve HTRB,
several strategies can be implemented, such as optimizing the design of the JFET region and implementing a deep P-well.

2.4.5. **Body Diode Degradation**

In power electronic applications, the internal body diode of 4H-SiC MOSFETs can be utilized as a free-wheeling diode. However, 4H-SiC MOSFETs face a critical issue concerning the degradation of the body diode. Despite significant reductions of Basal Plane Dislocations (BPDs) in both the 4H-SiC substrate and epitaxial layer, there still remain some BPDs that can affect the device’s performance after prolonged operation of the body diode.

In a study conducted by [53], [54], it has been reported that 4H-SiC MOSFETs exhibit body diode degradations after stress. When the p-n junction body diode is forward biased, electron-hole recombination takes place in the drift layer, providing energy to activate dislocation glide, which leads to the formation of stacking faults (SFs). The SFs manifest as triangular defects when
observed from the device’s surface, and their size is influenced by the thickness of the drift layer. Consequently, the carrier lifetime and mobility in 4H-SiC MOSFETs are reduced due to the activation of dislocation glide, resulting in the degradation of the conduction behavior in the 1\textsuperscript{st} and 3\textsuperscript{rd} quadrants. Additionally, the SFs introduce electronic states within the bandgap of 4H-SiC, which act as generation centers and reduce the lifetime, resulting in increased leakage current in the blocking mode under further stress [53].

Fig. 2.22 (a) illustrates the degradation of the 3\textsuperscript{rd} quadrant $I_D-V_D$ characteristics for the internal body diode before and after stress, with an $I_{DS}$ of -5 A and $V_{GS}$ of -5 V. Despite improvements in the quality of the epitaxial layer and the utilization of a thin epitaxial layer in the fabrication of 1.2 kV 4H-SiC MOSFETs, a slight degradation of the body diode has been observed.

To address the issue of body diode degradation, it is crucial to suppress bipolar operation. This can be achieved by utilizing MOSFETs with integrated channel diodes or junction barrier Schottky diodes, known as JBSFETs. These devices enable the unipolar operation and eliminate the need for reliance on the internal body diode [55]–[57]. By suppressing bipolar operation during the third quadrant characteristics, JBSFETs exhibited no degradation after stress measurements, as shown in Fig. 2.22 (b).

2.4.6. \textit{Short-Circuit Characteristics}

The occurrence of a short circuit in power electronic systems can be attributed to control errors or load failure, resulting in the formation of a low resistance path within the system. The fault current in power electronic systems is limited by the internal resistance of power semiconductor devices. Additionally, the duration for which the device can withstand the short
The trade-off relationship between specific on-resistance and short-circuit withstand time in 4H-SiC planar MOSFETs. The short-circuit characteristics were evaluated at $V_{gs}$ of 20 V and $V_{ds}$ of 800 V.

-circuit (SC) condition depends on the DC-link voltage applied across the device. When power semiconductor devices are exposed to currents significantly higher than their operating current and high DC-link voltage, they are subjected to high power dissipation, which can ultimately lead to device failure. Such failure can subsequently cause additional failures in system components. Therefore, the ability of power semiconductor devices to withstand short-circuit conditions for an extended period, known as the short-circuit withstand time (SCWT), is a critical factor in their suitability for use in power electronic applications.

The SC characteristics of 1.2 kV 4H-SiC MOSFETs are inferior to those of 1.2 kV Si IGBTs, primarily due to the combination of high maximum drain current and electric field across the drift region. The low specific on-resistance ($R_{on,sp}$) and high critical electric field of 4H-SiC MOSFETs contribute to these factors. Consequently, the high power dissipation results in elevated junction temperatures, leading to a reduction in the short-circuit withstand time of 4H-SiC MOSFETs.
The trade-off relationship between specific on-resistance and short-circuit withstand time in 4H-SiC trench MOSFETs with conventional, semi-superjunction, and full-superjunction \[71\]. The short-circuit characteristics were evaluated at \(V_{gs}\) of 20 V and \(V_{ds}\) of 600 V.

Various research groups have made efforts to enhance the short-circuit characteristics of 4H-SiC MOSFETs, but they encounter limitations due to the trade-off between \(R_{on,sp}\) and SCWT. Proposed approaches include reducing channel/JFET density, decreasing source doping, and lowering the gate voltage to improve SC characteristics \[61\]–\[64\]. However, these methods tend to increase \(R_{on,sp}\) while improving SCWT.

To overcome the conventional trade-off relationship between \(R_{on,sp}\) and SCWT, a narrow JFET width with an enhanced JFET doping concentration and a deep P-well structure can be utilized. These design modifications help suppress the maximum drain current during SC conditions, thereby addressing the trade-off issue.

Fig. 2.23 shows the trade-off relationship between specific on-resistance and short-circuit withstand time in 4H-SiC planar MOSFETs \[45\], \[58\], \[65-70\]. Group 2 exhibits a superior trade-off relationship compared Group 1, thanks to well-optimized cell structures and processes.
However, Group 3, which employs the deep P-well structure, achieves improved trade-off relationship [69], [70]. To further enhance this trade-off relationship, the utilization of superjunction (SJ) technology can be utilized.

Fig. 2.24 depicts the trade-off relationship between specific on-resistance and short-circuit withstand time in 4H-SiC trench MOSFETs with conventional, semi-SJ, and full-SJ [71]. Trench MOSFETs, owing to their high channel mobility, offer improved specific on-resistance. Additionally, the long short-circuit withstand time observed in Fig. 2.24 can be attributed to the utilization of low drain voltages during the short-circuit measurements. Notably, it was discovered that both the semi-SJ and full-SJ provide a significantly enhanced trade-off relationship.

2.5. REFERENCES


Chapter 3

Optimization of JFET and P-well Implantation for 1.2 kV 4H-SiC MOSFETs

3.1. INTRODUCTION

4H-SiC MOSFETs offer high breakdown voltage (BV), low specific on-resistance ($R_{on,sp}$), and fast switching speed when compared with Si IGBTs [1]. Especially, 1.2 kV rated MOSFETs have been developed for utilization in hybrid electric vehicles (HEV) and pure electric vehicles (EV). In order to improve the characteristics of 1.2 kV SiC MOSFETs, various processes and designs have been reported. Due to the prevalent SiO$_2$/SiC interface traps and the resultant low channel mobility, most of the development in SiC MOSFETs has focused on reducing channel resistance [2–5]. In [6–8], the importance of JFET resistance in the DMOSFETs has been reported. Even though JFET design largely affects the characteristics of the MOSFETs as much as channel parameters do [9], the importance of the JFET and P-well implants has not been inclusively discussed; Especially, detailed research on the effect of depth of JFET and P-well implants has been lacking. In addition, the impact of the high channel mobility on the short-circuit characteristics hasn’t been reported.

In this paper, the influence of deep JFET and P-well implants in 1.2 kV MOSFETs was investigated with respect to static characteristics and short-circuit ruggedness. 4H-SiC MOSFETs with nominal implants for JFET and P-well, deep JFET implants, and deep P-well implants have been successfully fabricated and evaluated on a 6-inch SiC substrate. Channel lengths and JFET widths were varied to compare the depth of implants for JFET and P-well on performance outcomes and short-circuit ruggedness. For short-circuit characteristics, the effect of the channel
Fig. 3.1. The schematic cross-sectional views of 1.2 kV MOSFETs with (a) nominal implants, (b) deep JFET implants, and (c) deep P-well implants.

Fig. 3.2. The cross-sectional SEM images of the fabricated 1.2 kV 4H-SiC MOSFETs with $L_{ch}$ of 0.5 µm and $W_{JFET}$ of 0.8 µm for (a) nominal, (b) deep JFET, and (c) deep P-well implants.

Mobility was also examined. In order to understand this influence, Sentaurus 2D-simulations were used.

### 3.2. Device Design

Fig. 3.1 (a), (b), and (c) show the schematic cross-sectional views of MOSFETs with nominal implants, deep JFET implants, and deep P-well implants, respectively. The depth of JFET/P-well...
was designed to be approximately 0.6/0.7, 0.9/0.7, and 0.9/1.1 μm, for nominal, deep JFET, and deep P-well implants, respectively.

The optimization of the channel region is inevitable for 1.2 kV-rated 4H-SiC MOSFETs due to the high proportion of the channel resistance out of total on-resistance. In parallel with the effort of improving channel mobility, the implementation of a short channel length is preferable. However, the reduced channel length would increase the leakage current under the blocking mode of operation [9]. As the design of JFET/P-well and its resultant static/ruggedness performances are closely linked with the channel design as well, various channel lengths ($L_{ch} = 0.3, 0.4, and 0.5 \mu m$) with half-JFET width ($W_{JFET}$) of 0.8 μm were fabricated.

In addition, the optimization of the JFET region is crucial as it determines not only the specific on-resistance, but also the leakage current and short-circuit withstand time (SCWT) [9], [10]. On the one hand, the deep JFET structure, combined with enhanced doping, enables the JFET width to be narrowed while enhancing conduction performance without compromising blocking behavior. Also, deep JFET, implementing a current spreading layer (CSL), provides additional improvement in forward conduction due to low JFET resistance. On the other hand, a deep P-well, shielding the channel better from high drain bias, would improve blocking behavior and SCWT, but causes $R_{on,sp}$ to increase requiring a wider JFET width. To find the optimum cell design for deep JFET or P-well structures, different half-JFET widths ($W_{JFET} = 0.6, 0.7, 0.8, and 0.9 \mu m$) with $L_{ch}$ of 0.5 μm were fabricated.

To effectively evaluate the proposed structures, an efficient and stable (against process conditions) edge termination structure is required. A Hybrid-junction termination extension (Hybrid-JTE) was designed to achieve near-ideal blocking behaviors [11].
3.3. DEVICE FABRICATION TECHNOLOGY

The devices were fabricated at Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, US. [9]. For the implementation of the different JFET and P-well implants, three wafers were fabricated using the same process baseline. Various designs of MOSFETs with $W_{\text{JFET}} = 0.6, 0.7, 0.8, \text{ and } 0.9 \ \mu\text{m and } L_{\text{ch}} = 0.3, 0.4, \text{ and } 0.5 \ \mu\text{m were included in the same mask set. A 10 \ \mu\text{m thick drift layer with N- epi doping concentration of about } 8\times10^{15} \ \text{cm}^{-3} \text{ on a 6-inch, N+ 4H-SiC substrate was used for the fabrication of } 1.2 \ \text{kV MOSFETs. Aluminum and Nitrogen ion implants were utilized to form P-well/P+body/JTE, and JFET/N+ source, respectively. JFET and P-well profiles were designed to achieve an accumulation mode channel for higher channel mobility [3]. After implantation steps, a } 1650 \ ^\circ\text{C 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed by } 800 \ ^\circ\text{C ultrathin thermal oxide (2 nm) with 48 nm of deposited oxide, followed by a post oxidation anneal (POA) in N}_2\text{O ambient to improve the channel mobility. The N-type polysilicon was deposited and patterned for the formation of the gate. After interlayer dielectric (ILD) was deposited, patterned, and etched to make ohmic contact regions, Nickel (Ni) was deposited on the front side, followed by rapid thermal annealing (RTA) for the self-aligned silicidation process. Next, unsilicided Ni metals were removed and annealed by a 2 minute RTA at } 965 \ ^\circ\text{C for the front side ohmic contact. Backside metal was also deposited by Ni, followed by the same RTA process. A 4\mu\text{m thick Ti/TiN/Al was deposited as the source and the gate metal. Silicon nitride and polyimide were used for passivation on the frontside. Finally, a solderable metal stack was deposited on the backside. No substrate thinning process was adopted. Fig. 3.2 shows the cross-sectional scanning electron microscope (SEM) images of the fabricated MOSFETs for nominal, deep JFET, and deep P-well implants.}
3.4. RESULTS AND DISCUSSIONS

3.4.1. JFET/P-WELL DESIGN VARIATIONS

Fig. 3.3 (a) shows output characteristics of the fabricated SiC MOSFETs with channel length ($L_{ch}$) of 0.5 µm and half-JFET width ($W_{JFET}$) of 0.8 µm. MOSFETs with different implant conditions were measured at gate-source biases of 0 to 20 V with 10 V steps. The specific on-resistance of the measured MOSFETs is extracted at gate-source biases ($V_{gs}$) of 20 V and drain-source biases ($V_{ds}$) of 0.1 V. For nominal, deep JFET, and deep P-well implant for MOSFETs with $L_{ch}$ of 0.5 µm and $W_{JFET}$ of 0.8 µm, the on-wafer level $R_{on,sp}$ are 4.68, 4.12, and 5.45 mΩ-cm$^2$, respectively. The difference in the conduction behaviors originates from the JFET resistance. The MOSFET with deep JFET offers a better conduction behavior due to reduced JFET resistance. As shown in Fig. 3.3 (b), regardless of implant profiles, short channel lengths provide lower specific on-resistance due to the reduction in channel resistance.

In order to clarify this behavior, Sentaurus 2D TCAD was used. Fig. 3.4 (a) shows the cross-sectional view of simulated 1.2 kV MOSFETs with $L_{ch}$ of 0.5 µm and $W_{JFET}$ of 0.8 µm. The simulated structures were configured based on the P-well and JFET implant profiles shown in Fig. 3.1 and Fig. 3.2. As previously mentioned, the JFET and P-well implants determine current conduction behaviors. 2D simulations clearly show how current density distributions are affected by deep JFET and P-well implants; Fig. 3.4 (b). Deep JFET implants contribute to the reduction in lateral and vertical depletion regions at the bottom of the P-well region, resulting in larger cross-sectional areas for electrons to flow (i.e. a CSL), which in turn generates lower specific on-resistance. Conversely, deep P-well implants cause an increase in depletion regions constricting the flow of electrons. When the JFET implant is deeper than the P-well implant, resulting in the removal of the vertical straggle of Aluminum, as shown in Fig. 3.4 (a), the significantly improved
Fig. 3.3. (a) Measured output characteristics of MOSFETs with $L_{ch}$ of 0.5 $\mu$m and $W_{JFET}$ of 0.8 $\mu$m with different implant conditions (room temperature), and (b) Summary of measured specific on-resistances depending on the channel length. It should be noted that all measurements were conducted on-wafer level and a 10 – 15% reduction in on-resistance is expected from packaged devices, according to our previous results.

Fig. 3.4. (a) The cross-sectional view of simulated 1.2 kV MOSFETs with $L_{ch}$ of 0.5 $\mu$m and $W_{JFET}$ of 0.8 $\mu$m. (b) Current density distribution in simulation at $V_{gs}$ of 20 V and $V_{ds}$=1 V.
conduction behaviors were achieved. It should be noted that JFET implants should be deeper than P-well implants in order for higher conduction behavior to be achieved.

3.4.2. JFET/P-well Design Variations with Different $L_{\text{Ch}}$

Fig. 3.5 shows the forward blocking behaviors of the fabricated MOSFETs with different channel lengths for different implant conditions. Regardless of implant condition, high blocking behaviors with a significantly low leakage current were achieved for all MOSFETs with a channel length of 0.5 $\mu$m. In contrast with the output characteristics, MOSFETs with shorter channel length have a deleterious effect on the blocking capability, resulting in the increase of leakage current and the reduction in breakdown voltage (BV) under the blocking mode. Breakdown of MOSFETs with shorter channel occurs due to the increase of leakage current originating from the channel, not as a result of avalanche breakdown. This is because, for a shorter channel, channel potential (potential barrier formed in the channel) easily collapses under the high drain voltages. However, deep P-well with shorter channel lengths provides higher breakdown voltage when compared with others because the channel is effectively protected (i.e. shielded) by the deep P-well, suppressing leakage current from the channel. Fig. 3.3 and Fig. 3.5 clearly demonstrate the trade-off relationship between $R_{\text{on,sp}}$ and BV in regards to the channel length and JFET/P-well depths.

In order to further explore the effect of channel length under the blocking mode, simulated electrostatic potential near the surface, starting at the N+ source, proceeding through the channel, and ending in the JFET region (A-A’ shown in Fig. 3.4) was extracted at $V_{\text{ds}}$ of 1500 V, as shown in Fig. 3.6 (a). Simulation demonstrates longer channel length has a larger and thicker potential barrier, thus providing lower leakage current. Based on Fig. 3.6 (a), channel potential was extracted at $V_{\text{ds}}$ of 1500 V to examine the impact of depth in JFET and P-well regions. As shown in Fig. 3.6
Fig. 3.5. Measured forward blocking behaviors of the fabricated MOSFETs with \( W_{\text{JFET}} \) of 0.8 \( \mu \text{m} \) and different channel lengths.

(b), in contrast with the output characteristics, deep P-well allows the improved characteristics under the blocking mode due to a larger depletion region in the JFET region that effectively shields the channel, resulting in a higher channel potential. Furthermore, for MOSFETs with deep P-well, the change in channel potential with respect to channel length remains the lowest, as observed by...
comparing the slopes of the lines plotted in Fig. 3.6 (b). These results mean that MOSFETs with deep P-well allow the use of a short channel length of 0.4 µm to achieve lower on-resistance while maintaining low leakage current and high breakdown voltage. Moreover, it is useful in creating a more robust and forgiving MOSFET fabrication process, as any resulting channel length imbalances due to misalignment between P-well and N+ source implants do not produce the same negative performance outcomes typically observed when using the nominal MOSFET structure. It should be noted that here channel misalignment refers to one side of the MOSFET unit-cell having a channel length that is shorter, and the other side having a channel length that is longer, than the designed channel length. Therefore, the blocking behavior of the nominal MOSFET structure is dictated by the length of the shorter side of the channel; a problem less prominent when implementing a deep P-well.

3.4.3. JFET/P-well Design Variations with Different W_{JFET}

In order to further examine the impact of JFET and P-well implants, MOSFETs with W_{JFET} of 0.6, 0.7, 0.8, and 0.9 µm were also fabricated on the same mask set. Fig. 3.7 (a) shows output characteristics of the fabricated MOSFETs with nominal implant (L_{ch} = 0.5 µm) using different JFET widths. The conduction behaviors increase, resulting in low R_{on,sp} when JFET width increases. The difference in the R_{on,sp} originates from JFET resistance. In Fig. 3.7 (b), the impact of deep JFET and deep P-well on R_{on,sp} is also observed. The optimum JFET width for the deep P-well structure is much larger than the one for the deep JFET structure. This is due to the difference in the effective JFET width despite the same designed W_{JFET}. The deep P-well has a large lateral straggle due to the high energy implantation, causing the narrow effective JFET width, as shown in Fig. 3.8. Moreover, a large depletion region occurs in the deep P-well, reducing the
Fig. 3.7. (a) Measured output characteristics of the fabricated MOSFETs with nominal implant and different JFET widths ($L_{ch}=0.5 \ \mu m$). (b) Summary of specific on-resistance with different implant conditions depending on JFET width.

Fig. 3.8. (a) The cross-sectional SEM image of the fabricated 1.2 kV 4H-SiC MOSFETs with $L_{ch}$ of 0.5 $\mu m$ and $W_{JFET}$ of 0.8 $\mu m$ for (a) nominal and (b) deep P-well implants.

effective JFET width and increasing the JFET depth, as shown in Fig. 3.4 (b). It is important to note that the depth of both JFET and P-well is considered when optimizing JFET width; Narrow JFET width with deep JFET implants can be designed to improve BV with no negative impact on $R_{on,sp}$. For a deep P-well structure, a wide JFET region is required to provide low specific on-resistance.
Fig. 3.9. (a) Measured forward blocking behaviors of the fabricated MOSFETs with nominal implant and different JFET widths ($L_{ch}=0.5 \ \mu m$). (b) Summary of measured breakdown voltage and simulated channel potential at $V_{ds}$ of 1500 V with different implant conditions depending on JFET width.

Fig. 3.9 (a) shows measured forward blocking characteristics, for various JFET widths of the fabricated MOSFETs with nominal implants. Regardless of JFET width, significantly low leakage current and high breakdown voltage were achieved. In contrast with MOSFETs with shorter channel ($L_{ch} = 0.3$ and $0.4 \ \mu m$), MOSFETs with varied JFET widths provide high breakdown voltage with low leakage current due to longer channel length ($L_{ch} = 0.5 \ \mu m$). When channel potential is high enough to suppress the leakage current through the channel under the high drain voltages, avalanche breakdown generally becomes dominant. Furthermore, as shown in Fig. 3.9 (b), regardless of implant condition, breakdown voltage increases when JFET width decreases; with breakdown occurring at the edge of the P-well. Narrow JFET width provides a greater shielding effect between P-wells, contributing to high breakdown voltage. It is important to note that change in BV as a function of JFET width is small for deep P-well structure due to the narrow effective JFET width, as shown in Fig. 3.4 (b). However, when compared with other implant conditions, the BV of MOSFETs with deep P-well slightly decreases due to the reduction in the
The depth of implants regarding different JFET widths was also studied using 2D-simulation. The decreased JFET width provides the increase in channel potential, as shown in Fig. 3.9 (b). It is also demonstrated that a deep P-well structure enables high channel potential due to its better shielding effect. When a shorter channel is required to improve the forward conduction, a deep P-well structure and narrow JFET width are suitable to suppress the leakage current under the blocking mode.

3.4.4. TRADE-OFF BETWEEN $R_{ON,SP}$ – SCWT AND DISCUSSION

The short-circuit waveforms of the fabricated MOSFETs with $W_{JFET}$ of 0.6 µm using nominal implant are shown in Fig. 3.10 (a). The measurement for short-circuit was conducted under the following conditions: $R_g$ of 20 Ω, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V at room temperature. Fig. 3.10 (b) shows the drain current of fabricated MOSFETs with different gate pulse widths until the devices failed. At the beginning of the short-circuit condition, the maximum drain current ($I_{max}$) occurs, causing the increase of junction temperature. Next, the drain current starts decreasing because of the decrease in electron mobility at high temperatures. The simulated drain current of MOSFETs is shown in Fig. 3.10 (c). Thanks to the well-optimized thermal-related simulation models [10], the simulated SCWT well corresponds with the experimental SCWT. Fig. 3.11 (a) shows the drain current of the fabricated MOSFETs with $W_{JFET}$ width of 0.6 µm using different implants. It shows that short-circuit withstand time is determined by $I_{max}$; low $I_{max}$ results in low junction temperatures, offering long SCWT. The difference in $I_{max}$ originates from the JFET region (resistance). As mentioned in forward characteristics, different JFET and P-well implants contribute to the different effective JFET widths despite the same designed JFET width.
Fig. 3.10. (a) Measured short-circuit waveforms of the fabricated MOSFETs with nominal implant (W_{JFET} of 0.6 µm and L_{ch} of 0.5 µm). (b) Measured drain current of the fabricated MOSFETs (W_{JFET} of 0.6 µm and L_{ch} of 0.5 µm) with different gate pulse widths under SC condition. (c) Simulated drain current of MOSFETs (W_{JFET} of 0.6 µm and L_{ch} of 0.5 µm) with different gate pulse widths under SC condition.

Fig. 3.11. Measured drain current of the fabricated MOSFETs with (a) different implants (W_{JFET} of 0.6 µm and L_{ch} of 0.5 µm) and (b) JFET widths (deep JFET implant). SC condition was R_g of 20 Ω, V_{gs} of 20 V, and V_{ds} of 800 V.
Fig. 3.12. (a) Summary of simulated trade-off relationship between $R_{on,sp}$ and SCWT depending on different implants with different JFET widths. (b) The cross-sectional view of simulated 1.2 kV MOSFETs with deep JFET and P-well implant. (c) Designed implant profiles for channel region and P-well (B-B’) using SPROCESS.

Especially, under SC condition that is extremely high temperatures, the maximum saturation current is largely affected by the effective JFET width [12]. The drain current of the fabricated MOSFETs with different JFET widths using deep JFET implants is shown in Fig. 3.11 (b). In the same manner as different implants, narrow JFET width provides low $I_{max}$, resulting in long SCWT.

Fig. 3.12 (a) summarizes the simulated trade-off relationship between $R_{on,sp}$ and SCWT depending on the different implants with different JFET widths. It clearly shows MOSFETs have
Summary of the simulated trade-off relationship between $R_{on,sp}$ and SCWT depending on different implants with different channel lengths is shown in Fig. 3.13 (a). MOSFETs with deep JFET implant show a better trade-off relationship when compared to MOSFETs with nominal implant and deep P-well implant.

Summary of the simulated trade-off relationship between $R_{on,sp}$ and SCWT depending on different implants with different channel lengths is shown in Fig. 3.13 (a). MOSFETs with deep JFET implant show a better trade-off relationship when compared to MOSFETs with nominal implant and deep P-well implant.

Fig. 3.13. Summary of simulated trade-off relationship between $R_{on,sp}$ and SCWT depending on (a) different implants with different channel lengths (b) different JFET widths and different channel lengths with different channel mobilities for MOSFETs with deep JFET implant.

trade-off relationship between $R_{on,sp}$ and SCWT regardless of the implant condition. Although deep P-well implant has long SCWT due to high $R_{on,sp}$, the deep JFET implant exhibits the better trade-off relationship because of the feasibility of narrow JFET width. Fig. 3.12 (b) shows the cross-sectional view of simulated 1.2 kV MOSFETs with the deep JFET and P-well implant. MOSFETs with the deep JFET and P-well implant are conducted to improve SC characteristics. For MOSFETs with the deep JFET and P-well, the depth of JFET and P-well was designed to be approximately 1.3 μm and 1.1 μm, respectively. Fig. 3.12 (c) shows the designed implant profiles for the channel region and P-well using SPROCESS [13]. It is discovered that MOSFETs with the deep JFET and P-well implant provide much-improved trade-off relationship.

Summary of the simulated trade-off relationship between $R_{on,sp}$ and SCWT depending on different implants with different channel lengths is shown in Fig. 3.13 (a). MOSFETs with deep JFET implant show a better trade-off relationship when compared to MOSFETs with nominal implant and deep P-well implant.
different JFET widths and channel lengths with different channel mobilities is shown in Fig. 3.13 (b). The change of JFET width provides a better trade-off relationship when compared to that of channel length using the current channel mobility of 20 cm²/V·s. This is because the low channel mobility results in a large increase in the channel resistance with increasing channel length. However, the increased channel mobility significantly improves the trade-off relationship. This is attributed to the temperature dependence of channel mobility. The channel mobility at low temperatures, which is less than 200 °C, is determined by the interface trap [14]. However, at high temperatures, phonon scattering becomes dominant in determining channel mobility [14]. The channel mobility at high temperatures is almost identical regardless of whether the channel mobility is low or high at low temperatures. Therefore, the high channel mobility provides low \( R_{\text{on},sp} \) with almost no negative impact on SCWT. The long channel length with high channel mobility would offer improved short-circuit characteristics without the degradation of conduction behaviors. It is discovered that high channel mobility improves forward conduction performances as well as short-circuit characteristics.

Table 3.1 summarizes the experimental and simulated results. MOSFETs with deep JFET implant provide the low \( R_{\text{on},sp} \) with high breakdown voltages. SCWT increases by using a deep P-well implant. However, the deep JFET implant exhibits a better trade-off relationship between \( R_{\text{on},sp} \) and SC.
3.5. CONCLUSION

The effect of the depth of JFET and P-well implants was examined in terms of the trade-off relationship between $R_{on,sp}$ and BV or SCWT in the 1.2 kV 4H-SiC MOSFETs. These trade-offs are successfully demonstrated by comparing the 1.2 kV MOSFETs with different JFET widths and channel lengths. The forward conduction mode, blocking behaviors, and short-circuit characteristics of the fabricated MOSFETs are evaluated. In order to clearly understand and clarify experimental results, 2D-simulation results were included, as well. Deep JFET implants provide a significantly improved forward conduction mode when compared with nominal implants. In contrast, deep P-well implants allow a low leakage current and high breakdown voltage for structures with even shorter channel length. Moreover, MOSFETs with deep P-well implant have long SCWT because of high $R_{on,sp}$. However, the deep JFET implant provides a better trade-off relationship between $R_{on,sp}$ and SCWT due to the utilization of narrow JFET width. Finally, the change of JFET width and channel length with different channel mobilities was discussed. The MOSFETs with the deep JFET and P-well implant are proposed to improve trade-off relationship between $R_{on,sp}$ and SCWT. It is important to note that high channel mobility is required to improve not only static characteristics but also short-circuit characteristics. Based on the application of the 1.2 kV MOSFETs, the design and process of MOSFETs need to be carefully optimized due to the trade-off between $R_{on,sp}$ and BV or SCWT.

3.6. ACKNOWLEDGMENT

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3.7. REFERENCES


Chapter 4

Analysis for the Cell Design of 1.2 kV 4H-SiC Planar MOSFETs

4.1. INTRODUCTION

Silicon Carbide (SiC) MOSFETs provide various advantages for high voltage and high frequency applications, such as power inverter and fast charter for electric vehicles, medium voltage motor drives, and commercial aviation. In most applications, the driving force for the commercialization of SiC MOSFETs is low on-resistance with superior switching performance when compared to the Silicon IGBT. Numerous research efforts have been conducted aiming to minimize the specific on-resistance ($R_{on,sp}$) for a specified breakdown voltage (BV). The process technologies that enabled the demonstration of high-performance 1.2 kV SiC MOSFETs include the post oxidation anneal in nitric oxide (NO) [1], high quality epi-growth technique [2], ion implantations at elevated temperatures [3], etc. In regards to the device architecture, many groups have been developing the trench-type MOSFET [4], [5], but the planar-type MOSFET has remained mainstream since its commercialization in the early 2010s. Many novel design approaches, as well as edge termination techniques, for SiC planar MOSFETs have been attempted to improve $R_{on,sp}$, BV, switching performance, reliability, and the trade-offs between them. Accumulation mode channel has been reported to improve $R_{on,sp}$ due to the increase of channel mobility [6–8]. K. Han has reported the effect of channel length for the inversion mode channel MOSFETs [9]. The optimization of the JFET region [10] and current spreading layer (CSL) [11] have been suggested for the improvement of the forward conduction mode. A. Saha [11] and Q. Liu [12] have briefly reported the effect of cell pitch for $R_{on,sp}$. Although accumulation mode
Fig. 4.1. (a) a layout approach of MOSFETs with linear striped P+, (b) a layout approach of MOSFETs were placed intermittently in the orthogonal direction. (c) A-A’ cross-sectional view of MOSFETs with linear striped P+, (d) B-B’ cross-sectional view of N+ source contact of MOSFETs were placed intermittently in the orthogonal direction, and (e) C-C’ cross-sectional view of P+ body contact of MOSFETs were placed intermittently in the orthogonal direction.

channel MOSFETs with CSL are known to exhibit a trade-off relationship between $R_{on,sp}$ and BV with respect to the channel and JFET region, detailed information and discussion on the impact of the channel and JFET design for accumulation mode channel MOSFETs with CSL are lacking in previous literatures. Moreover, the completed and specific unit cell design rules are deficient, resulting in the lack of detailed research and comprehensive understanding regarding trade-off
relationship between \( R_{on,sp} \) and \( BV \) within the cell structure. In particular, when reviewing the presently available literature it is difficult to fairly compare the effect of each component of the MOSFETs due to different structures and processes reported by different groups. This study is particularly important for low voltage (600 ~ 1200 V) SiC MOSFETs because the on-resistance is largely dependent on the cell design.

This paper presents a comprehensive analysis of trade-off relationship between \( R_{on,sp} \) and \( BV \) (along with yield) for the 1.2 kV accumulation mode channel SiC MOSFETs with CSL and different dimensions in the cell structure. Such dimensions explored include, the channel, JFET, contact opening, ILD (inter-layer dielectric) width, and gate-to-source overlap. In order to conduct a completed experiment that produces comprehensive results for a deep understanding, while fairly comparing the effect of each component of the MOSFET, the 1.2 kV accumulation mode channel SiC MOSFET devices investigated in this paper were fabricated on the same, 6-inch wafer using the same mask set. In section II – Device Design, design approaches for the fabricated 1.2 kV SiC MOSFETs are discussed; In section III – Fabrication Technology, device fabrication process is
explained; In section IV – Results, electrical characteristics measured from fabricated SiC MOSFETs with the above mentioned design variations are presented; In section V – Discussions, inclusive analyses are provided.

4.2. DEVICE DESIGN AND MODELLING

Fig. 4.1 (a) and (b) show top views of layout designs for 1.2 kV SiC MOSFET cells with P+ sources located in a stripe pattern and intermittently located in the orthogonal direction, respectively. A-A’ cross-sectional view for the stripe pattern P+ is shown in Fig. 4.1 (c). In order to reduce dead space (i.e. the area underneath the P-well that is not fully utilized for the current conduction), and thus enable a reduction in the cell pitch, the P+ source contacts are intermittently placed in the orthogonal direction, as shown in Fig. 4.1 (b) [7]. Fig. 4.1 (d) and (e) pertain to the MOSFET with orthogonal P+ sources and show the cross-sectional views of portions that include N+ source contact and P+ source contact, respectively. As shown in Fig. 4.2, ion implantation schedules for the JFET region and P-well are designed to create the accumulation mode channel to attain high channel mobility [7]. A current spreading layer (CSL) underneath the P-well is adopted to further reduce the resistance near the bottom of the P-well. The half-cell pitch (A-A’ or B-B’) consists of contact opening (W_C), ILD width (W_{ILD}), gate-source overlap (W_{G-S}), channel length (L_{ch}), and JFET width (W_{JFET}), as shown in Fig. 4.1 (c). Analyses of device designs (described in Sections IV and V, with Table 4.1 containing detailed design parameters) were divided into 4 parts: contact opening, JFET width, channel length, and others (i.e. contact opening, ILD width, and gate-source overlap that determine the cell pitch altogether).

For fair evaluation in the blocking mode, an efficient edge termination structure is necessary to compare all the design variations mentioned above. A hybrid-junction termination extension
(Hybrid-JTE) was employed to achieve a near-ideal breakdown voltage [13].

Sentaurus 2D TCAD was used to support and clarify the experimental results. For the simulation of forward conduction, the Lombardi model for interface trap and channel mobility degradation was applied to match experimental channel mobility and $V_{th}$ [14–16]. The Okuto-Crowell model was used for the avalanche model [14], [17]. The BV value was extracted when the integral of impact ionization coefficient of holes reaches unity, which implies avalanche breakdown. Simulation models for Silicon Carbide have been developed and optimized [14], [18].

4.3. DEVICE FABRICATION TECHNOLOGY

The devices were fabricated by Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, using the same base process line [19], [20]. A 10 µm thick drift layer with N-type
doping concentration of $8\times10^{15}$ cm$^{-3}$ on 6-inch, N+ 4H-SiC substrate was used for the fabrication of proposed 1.2 kV MOSFETs. Aluminum and Nitrogen ion implants were used to form P-well/P+ source/JTE, and JFET/N+ source, respectively. All implants were conducted at 500 °C. After all implantation steps, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed by ultrathin (2 nm) thermal oxide and 48 nm of deposited oxide, followed by a post oxidation anneal (POA) in N$_2$O ambient. The N-type polysilicon was deposited and patterned for the formation of the gate. After, undoped silicon glass (USG) was deposited as interlayer dielectric (ILD), then patterned and etched to make ohmic contact regions. Nickel (Ni) was deposited on the frontside, followed by an RTA for the silicidation process. Next, unsilicided Ni metals were removed and annealed by RTA at 965 °C for 2 mins. The backside was then deposited by Ni, followed by the same RTA process. A 4 μm thick Ti/TiN/Al stack was deposited for the source and gate metal. Silicon nitride and polyimide were used for passivation. Finally, a solderable metal stack was deposited on the backside. Fig. 4.3 shows the cross-sectional SEM image of the fabricated MOSFET.

4.4. RESULTS

4.4.1. CONTACT OPENING ($W_C$)

To examine the impact of contact dimensions on the on-resistance, half contact openings ($W_C$) of 1.0, 0.5, 0.4, and 0.3 μm were included keeping other parameters identical ($W_{ILD}=0.6$ μm, $W_{GS}=0.5$ μm, $L_{ch}=0.5$ μm, and $W_{JFET}=0.8$ μm). Except for the structure with $W_C$ of 1.0 μm, all other MOSFETs used the design approach, as shown in Fig. 4.1 (b) to reduce the cell pitch. The resultant cell pitches are 6.8, 5.8, 5.6, and 5.4 μm, respectively.

Fig. 4.4 (a) shows output characteristics of the fabricated 1.2 kV rated SiC MOSFETs with
Fig. 4.4. (a) Output characteristics of fabricated 1.2 kV MOSFET with different \( W_C \) and (b) summary of experimental and simulated \( R_{on,sp} \). MOSFETs were measured at gate-source biases of 0 to 20 V with 10 V steps. The \( R_{on,sp} \) were extracted at \( V_{gs} \) of 20 V and \( V_{ds} \) of 0.1 V.

Fig. 4.5. (a) Measured transfer characteristics and (b) measured forward blocking behaviors of the fabricated MOSFETs with different \( W_C \).

different \( W_C \). All electrical data presented in this paper were measured from on-wafer. In our experience, after packaging, there is a 15% reduction in \( R_{on,sp} \). Structures with orthogonal P+ provide larger currents than the ones with stripe pattern P+ and \( W_C \) of 1.0 \( \mu \)m. This difference in the on-resistances originates from the cell pitch. The role of P+ source contact is to provide a stable zero potential to the P-well under the forward conduction mode. Both structures with striped and
orthogonal P+ sources successfully serve this purpose. However, the larger cell pitch in the stripe pattern MOSFET causes the increase in \( R_{on,sp} \). In contrast, MOSFETs with \( W_C \) of 0.5, 0.4, and 0.3 \( \mu m \) show identical output characteristics regardless of the cell pitch. The smaller \( W_C \) would increase N+ contact resistance in MOSFETs. This increase in N+ contact resistance is compensated by the decrease of resistance stemming from reducing the cell pitch. The measured specific contact resistance, extracted by N+ circular type transmission line measurements (cTLMs), was \( 6.18\times10^{-5} \, \Omega \cdot \text{cm}^2 \). Depending on the contact resistance, the optimum \( W_C \) will differ; When the specific contact resistance is much lower than \( 6.18\times10^{-5} \, \Omega \cdot \text{cm}^2 \), a tight \( W_C \) could reduce the on-resistance, although the degree of improvement would not be significant; The narrow \( W_C \) using ideal contact resistance which is zero provides the reduced \( R_{on,sp} \) in simulation, as shown in Fig. 4.4 (b).

The measured transfer characteristics of the fabricated MOSFETs with varied \( W_C \) are shown in Fig. 4.5 (a). The threshold voltage (\( V_{th} \)) extracted at drain-source current (\( I_{ds} \)) of 1 mA is about 2.6 V for all structures, which also highlights that the orthogonal direction P+ provides appropriate zero potential to P-well. Fig. 4.5 (b) shows measured forward blocking behaviors of the fabricated MOSFETs with different \( W_C \). Regardless of the split, high breakdown voltages with low leakage currents were accomplished thanks to the efficient edge termination technique (Hybrid-JTE). As expected, \( W_C \) for N+ is unrelated to blocking behaviors. It is important to note that orthogonal P+ design also provides a high breakdown voltage with no negative outcomes, such as snapback.

4.4.2. CHANNEL LENGTH (\( L_{CH} \))

The channel length (\( L_{ch} \)) was varied to investigate the trade-offs between \( R_{on,sp} \) and BV, and \( R_{on,sp} \) and \( V_{th} \). \( L_{ch} \) of 1.0, 0.5, 0.4, and 0.3 \( \mu m \) were designed keeping other design rules identical.
Fig. 4.6. The cross-sectional SEM image of the fabricated 1.2 kV 4H-SiC MOSFETs for the device of $L_{ch}$ of 0.5 μm.

Fig. 4.7. (a) Measured output characteristics of the fabricated MOSFETs with different $L_{ch}$ and (b) summary of experimental and simulated $R_{on,sp}$ with different channel mobilities (18, 36, and 54 cm²/V·s) and experimental $V_{th}$.

(W_c=0.5 μm, W_{ILD}=0.6 μm, W_{G,S}=0.5 μm, W_{JFET}=0.8 μm and orthogonal direction P+ were used).

Fig. 4.6 shows the cross-sectional SEM image of the accumulation mode channel MOSFET with $L_{ch}$=0.5 μm (showing C-C’ in Fig. 4.1 (e)). Accumulation mode channel was formed using the controlled JFET and P-well implants, as shown in Fig. 4.2.
Fig. 4.8. Measured transfer characteristics at $V_{ds}=0.1$ V and transconductances of the fabricated MOSFETs with different $L_{ch}$. $V_{th}$ were extracted from transfer characteristics at drain current of 1 mA. $V_{th}$, for $L_{ch}$ of 0.3, 0.4, 0.5, and 1.0 μm, are 2.2, 2.4, 2.6, and 3.2 V, respectively.

Fig. 4.7 (a) shows measured output characteristics of the fabricated accumulation mode channel MOSFETs with different $L_{ch}$. Due to lower channel resistance, shorter channels offer higher current at the same drain-source voltage. Another important variable along with the $L_{ch}$ is channel mobility. In this case, the field effect channel mobility extracted from a lateral test MOSFET (FATFET) with a $L_{ch}$ of 200 μm at $V_{ds}$ of 0.1 V was approximately 18 cm$^2$/V·s, which is considered as reasonable in the current SiC technology.

A summary of experimental and simulated $R_{on,sp}$ with different channel mobilities and experimental $V_{th}$ is shown in Fig. 4.7 (b). Simulated results with different channel mobilities show the importance of high channel mobility. As the channel mobility increases, the rate of change of $R_{on,sp}$ per increase of $L_{ch}$ gets smaller. The measured transfer characteristics and transconductance of the fabricated MOSFETs with different $L_{ch}$ are shown in Fig. 4.8. Transfer characteristics and transconductances were measured at $V_{ds}$ of 0.1 V. When compared with a longer $L_{ch}$, the transconductance of a shorter $L_{ch}$ decreases to a value of 0 much more dramatically after reaching the maximum transconductance value. As a result, a shorter $L_{ch}$ is preferred to minimize the
channel resistance and overall device on-resistance. However, the reduction in the on-resistance brings in a detrimental issue during the forward blocking mode.

Fig. 4.9 shows measured forward blocking behaviors of the fabricated 1.2 kV MOSFETs with various \( L_{ch} \); clearly showing that a shorter channel results in poor blocking behavior with large leakage current. Breakdown of MOSFETs with shorter channels (\( L_{ch} \) of 0.3 and 0.4 \( \mu \)m) occurs due to the increase of leakage current from the channel, not as a result of the avalanche breakdown. In contrast, the longer channel (\( L_{ch} \) of 0.5 and 1.0 \( \mu \)m) shows avalanche breakdown behaviors, identified by a sudden increase in the drain-source current. In order to further explore the effect of \( L_{ch} \) on the blocking behavior, simulated electrostatic potential near the surface, starting at the N+ source, proceeding through the channel, and ending in the JFET region (E-E’ shown in Fig. 4.10 (a)) was extracted at \( V_{ds} \) of 1500 V, as shown in Fig. 4.10 (b). It is demonstrated that longer \( L_{ch} \) has a larger and thicker potential barrier, thus providing lower leakage current under the high drain voltage. The large leakage current at low drain bias from the short channel structure originated from the reduced potential barrier formed across the channel. When the \( L_{ch} \) is sufficiently long (\( L_{ch} \geq 0.5 \mu \)m), the channel potential is maintained and blocks the leakage current between the source
and drain until the avalanche breakdown occurs.

Fig. 4.10 (c) summarizes the $R_{on,sp}$ and channel potential at $V_{ds}$ of 1500 V for simulated MOSFETs with varied $L_{ch}$. From the comparison between this simulation and experimental results (Fig. 4.9), it is concluded that a channel potential larger than at least 1.4 V is essential to suppress the leakage current up to the avalanche condition, which is informative when exploring new device design concepts using 2D device simulations.

It is particularly important to minimize the misalignment between P-well and N+ source since these two layers define the $L_{ch}$. With a certain misalignment, one side of the $L_{ch}$ in the unit cell structure, as shown in Fig. 4.10 (a), becomes smaller than the other resulting in large leakage current. To prevent both sides of the unit-cell from having a $L_{ch}$ shorter than the designed $L_{ch}$, alignment tolerance should be considered, and more preferably, a well-established process scheme to implement a self-align channel is required.
4.4.3. JFET WIDTH ($W_{\text{JFET}}$)

To optimize the JFET region, different $W_{\text{JFET}}$ of 0.6, 0.7, 0.8, and 0.9 μm were included. The designed doping concentration in the JFET region is approximately $3 \times 10^{16}$ cm$^{-3}$. The depth of the JFET junction is 0.9 μm and is 0.1 μm deeper than the P-well, which implements the current spreading layer (CSL). Enhanced doping in the JFET region with CSL allows a narrow $W_{\text{JFET}}$, which provides improved conduction and switching behaviors with reduced leakage current during the forward blocking mode. Fig. 4.11 (a) compares measurements and simulations of $R_{\text{on,sp}}$ for varied $W_{\text{JFET}}$. Simulation results agree well with the experimental data, regardless of the doping concentration in the JFET region. It was discovered that the enhanced doping in the JFET region allows significantly improved conduction behaviors. Fig. 4.11 (b) compares current density distributions of simulated MOSFETs with and without enhanced doping ($3 \times 10^{16}$ cm$^{-3}$) in the JFET regions ($W_{\text{JFET}}=0.7$ μm). Enhanced doping offers a larger effective $W_{\text{JFET}}$ for current to flow due to a smaller depletion region, enabling the use of narrower $W_{\text{JFET}}$ in design.

Fig. 4.12 (a) shows measured forward blocking behaviors of MOSFETs with varied $W_{\text{JFET}}$. Narrower $W_{\text{JFET}}$ provides higher breakdown voltage with lower leakage current because the channel is better shielded from the drain bias, as shown in Fig. 4.12 (b). Depending on the implementation of the JFET implant and doping concentration, the optimum $W_{\text{JFET}}$ will differ to achieve the best combination of low $R_{\text{on,sp}}$ with high breakdown voltage; the trade-off relationship between $R_{\text{on,sp}}$ and $BV$ was improved using JFET implant with CSL. Higher JFET doping is required to achieve narrower $W_{\text{JFET}}$ and therefore obtain the desired breakdown voltage, a lower electric field in the gate oxide, and improved short-circuit capability [21].
Fig. 4.11. (a) Summary of measured and simulated $R_{\text{on,sp}}$ and (b) current density distribution of simulated MOSFETs with $W_{\text{JFET}}$ of 0.7 µm (*Simulated JFET doping of $5 \times 10^{16}$ and $7 \times 10^{16}$ cm$^{-3}$ has channel doping of $3 \times 10^{16}$ cm$^{-3}$ to keep same channel region).
4.4.4. **CELL PITCH**

Different combinations of dimensions for the contact opening (W_C), ILD width (W_{ILD}), and G-S overlap (W_{G-S}) of 0.5/0.6/0.5, 0.4/0.4/0.3, 0.4/0.4/0.2, and 0.3/0.3/0.2 μm (L_{ch}= 0.4 μm and W_{JFET}= 0.8 μm) were included to examine the impact of the cell pitch on the R_{on,sp}. It is important to investigate the manufacturability of these structures since there are concerns regarding gate-to-source leakage and misalignments between different mask layers. Fig. 4.13 shows the measured R_{on,sp} from MOSFETs with different cell pitches. As expected, a smaller cell pitch is beneficial in reducing the R_{on,sp}. To suppress the leakage current and attain higher BV, simulated R_{on,sp} in the case of L_{ch}=0.5 μm are also added in Fig. 4.13. The difference between experimental and simulated results stems from the contact resistance, as mentioned in Section IV - A.

While pursuing a smaller cell pitch to reduce the R_{on,sp}, it is important to evaluate the yield loss due to the aggressive design rules for W_{ILD} and W_{G-S}. Too small W_{ILD} provokes shorting between gate and source, resulting in high gate leakage and low gate-source breakdown. In other
words, a tight $W_{ILD}$ has trouble with gate control. During the fabrication of SiC MOSFETs, misalignments between the N+ source implant and gate poly are inevitable, as shown in Fig. 4.14. When the N+ source and gate poly become significantly separated due to misalignment, MOSFETs
Fig. 4.15. (a) Wafer-map of extracted $R_{on,sp}$ from the MOSFETs with different cell pitch and (b) the percentage of yield issue for MOSFETs and $R_{on,sp}$ with varied cell pitch (G-S short: Gate voltage was not applied, High $R_{on,sp}$: when compared with cell pitch of 4.6 μm in the same die, $R_{on,sp}$ was higher).

ultimately lose one side of the channel within the unit cell, resulting in high $R_{on,sp}$. Fig. 4.15 (a) shows half-wafer maps measured from devices with different cell pitches demonstrating yield losses due to narrow $W_{ILD}$ and small $W_{G-S}$. Fig. 4.15 (b) summarizes the % yield losses based on the measurement shown in Fig. 4.15 (a). Cell pitch of 5.6 μm ($W_{ILD}=0.6$ μm, $W_{G-S}=0.5$ μm) has 100% operational yield. However, when reducing $W_{ILD}$ from 0.6 μm to 0.4 μm, several operational
failures occurred (i.e. 1 or 2 out of 15 have a problem with gate control). When $W_{ILD}$ becomes 0.3 μm, the gate failure rapidly increases (4 out of 15). Yet, a decreased $W_{G-S}$ of 0.5 to 0.3 μm resulted in a 100% operational yield. However, it was observed that a $W_{G-S}$ of 0.2 μm began to cause the loss of channel due to misalignment, resulting in the increase of $R_{on,sp}$ in spite of reduced cell pitch. It was discovered that tight cell pitch caused by tight $W_{ILD}$ and $W_{G-S}$ increases the likelihood of operational failure. $W_{ILD}$ of larger than 0.4 μm and $W_{G-S}$ of larger than 0.3 μm are required to operate MOSFETs without failure and achieve low yield losses.

4.5. DISCUSSIONS

Fig. 4.16 (a) summarizes $R_{on,sp}$ as a function of different dimensions in the MOSFET cell structure. Although improving the channel resistance has been the main focus of the SiC industry, the channel mobility for a planar-type MOSFET remains in the range of 15 – 30 cm$^2$/Vs. As a result, the channel resistance still contributes to the largest portion of $R_{on,sp}$ of 1.2 kV SiC planar MOSFET. With the aid of higher channel mobility, a three times higher channel mobility as an example, an 18% improvement in the $R_{on,sp}$ can be additionally achieved, as shown by the dashed line in Fig. 4.16 (a). In contrast, a small change of $R_{on,sp}$ between $W_{JFET}$ was achieved, even for a $W_{JFET}$ of 0.6 μm. However, $W_{JFET}$ smaller than 0.6 μm with the same doping concentration would dramatically increase the $R_{on,sp}$. Therefore, a further enhanced doping concentration in the JFET region can be considered to accomplish a narrower $W_{JFET}$ and further reduce $R_{on,sp}$ (see the dotted line). It is also important to note that reduced cell pitch associated with orthogonal P+ and tight $W_{ILD}$ and $W_{G-S}$ is proven to be effective in reducing $R_{on,sp}$ without negatively impacting the blocking behavior, at the price of serious device yield issues.

Figure-of-Merits (FOM, $BV^2/R_{on,sp}$) [22] are shown in Fig. 4.16 (b) to compare static
Fig. 4.16. (a) Summary of $R_{on,sp}$ and (b) FOM depending on delta dimension for each parameter (*Nominal device has $W_C=0.5 \, \mu m$, $L_{ch}=0.5 \, \mu m$, $W_{JFET}=0.8 \, \mu m$, and cell pitch=5.8 $\mu m$).

characteristics for each component. FOM exhibits strong sensitivity to $L_{ch}$ due to low channel mobility; the shorter channel has lower BV and the longer channel provides higher $R_{on,sp}$. The improved channel mobility is an effective way to further increase FOM as shown in the dashed line. For $W_{JFET}$ variations, FOM is relatively similar due to enhanced JFET implant with CSL. Depending on $W_C$ for N+, FOM is almost identical. In contrast, the change of $W_c$ of 1 $\mu m$ to 0.5
μm increases FOM because of the use of orthogonal P+ causing reduced cell pitch (W_C for N+ is the same). The decreased cell pitch caused by reduced WILD and W_G-S also increases FOM. However, when considering the yield issue, a cell pitch of 4.6 μm is seen as the optimum value.

Trendline for cell pitch for an Lch of 0.5 μm exhibits the improvement of static characteristics when compared with an Lch of 0.4 μm due to the high BV. In general, it was demonstrated that device performance is significantly affected by cell design when considering all aspects. Table 4.1 summarizes all experimental results and design information. It was discovered that Lch is the most critical factor for the Ron,sp, resulting in 0.364 mΩ-cm² increase per 0.1 μm increase in Lch (ARon,sp / Δdimension). Reducing the cell pitch by putting the p+ source in the orthogonal direction results in a greater influence on the Ron,sp change than by controlling WILD and/or W_G-S. The optimization of the JFET region parameters is also very important but would produce an opposite trend when doping is further enhanced. Combined efforts to improve the channel mobility and enhanced doping in the JFET region will benefit all aspects of SiC MOSFETs.

<table>
<thead>
<tr>
<th>Device Structure</th>
<th>Experimental results</th>
<th>Design information</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Ron,sp [mΩ-cm²]</td>
<td>Vth [V]</td>
</tr>
<tr>
<td>W_C=1.0 μm</td>
<td>4.64</td>
<td>2.6</td>
</tr>
<tr>
<td>W_C=0.5 μm</td>
<td>4.11</td>
<td>2.6</td>
</tr>
<tr>
<td>W_C=0.4 μm</td>
<td>4.13</td>
<td>2.6</td>
</tr>
<tr>
<td>L_JFET=1.0 μm</td>
<td>6.11</td>
<td>3.2</td>
</tr>
<tr>
<td>L_JFET=0.5 μm</td>
<td>4.11</td>
<td>2.6</td>
</tr>
<tr>
<td>L_JFET=0.4 μm</td>
<td>3.84</td>
<td>2.4</td>
</tr>
<tr>
<td>L_JFET=0.3 μm</td>
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<tr>
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</tr>
<tr>
<td>W_JFET=0.6 μm</td>
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<td>2.6</td>
</tr>
<tr>
<td>Cell pitch=5.6 μm</td>
<td>3.84</td>
<td>2.4</td>
</tr>
<tr>
<td>Cell pitch=4.6 μm</td>
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<td>2.4</td>
</tr>
<tr>
<td>Cell pitch=4.4 μm</td>
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</tr>
<tr>
<td>Cell pitch=4.0 μm</td>
<td>3.37</td>
<td>2.4</td>
</tr>
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</table>
4.6. CONCLUSION

The fabricated 1.2 kV 4H-SiC MOSFETs with accumulation mode channel are closely investigated in terms of all aspects of design ($W_C$, $W_{ILD}$, $W_{G-S}$, $L_{ch}$, and $W_{JFET}$) on static characteristics, such as output and transfer characteristics, and blocking behaviors. Moreover, 2D-simulation was implemented to elucidate the effect of cell design from experimental results and suggest a direction to be further improved. It is demonstrated that $L_{ch}$ is the most critical factor in 1.2 kV 4H-SiC MOSFETs due to low channel mobility; 3 times channel mobility can improve $R_{on,sp}$ of 18% with no negative effect on BV. The enhanced JFET doping with CSL allows lower $R_{on,sp}$, and narrow $W_{JFET}$, providing better blocking and reliability; to further improve the device performance and reliability, the increased JFET doping with narrower $W_{JFET}$ is preferable. Different $W_c$ exhibits identical static characteristics in low contact resistance; when contact resistance is near ideal, narrower $W_c$ provides better conduction behaviors due to tight cell pitch. Lastly, the reduced cell pitch from tight $W_C$, $W_{ILD}$, and $W_{G-S}$ reduces $R_{on,sp}$ without negatively affecting blocking behaviors, but too tight $W_{ILD}$ and $W_{G-S}$ trigger operational failures. Overall, a detailed structural analysis of 1.2 kV 4H-SiC MOSFETs with accumulation mode channel enables further device performance improvements to be proposed.

4.7. ACKNOWLEDGMENT

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Chapter 5

Optimization of 1.2 kV 4H-SiC MOSFETs for Enhanced Short-Circuit Ruggedness using Non-Isothermal Simulations

5.1. INTRODUCTION

Although 4H-SiC MOSFETs are widely used in power electronics applications, detailed research on short-circuit failure mechanisms and device optimization based on device simulations is lacking. Generally, SC failure mechanisms for SiC MOSFETs can be categorized into three (Gate failure, Al melting, and thermal generated current) [1–3]. However, it is not obvious which mechanism dominates the short-circuit capability. Source doping reduction, lower channel density, and use of lower gate bias have been proposed to enhance SC capability [4]. However, these approaches result in the increase in $R_{on,sp}$. In comparison, SiC MOSFETs with reduced gate oxide thickness ($t_{ox}$) have demonstrated reduced saturation current ($I_{sat}$), with no impact on $R_{on,sp}$ [5], [6].

In this paper, firstly, failure mechanisms for short-circuit are investigated. In order to precisely analyze the device structure, thermal-related simulation models are covered. The effect of thin gate oxide on SC capability has been studied in depth using Non-Isothermal device simulations. In addition, a novel approach to improve both short-circuit withstanding time and static performance, when compared to reduced gate oxide thickness, is proposed using a decreased JFET region width with increasing JFET doping concentration.

5.2. SHORT-CIRCUIT FAILURE MECHANISMS
During the short-circuit conditions, three separate phenomena might occur when a device fails. In the first failure type (gate failure), the device undergoes gate failure due to the increase in Fowler-Nordheim (FN) tunneling, contributing to high gate leakage current at high temperatures. Furthermore, when gate oxide is exposed to high temperatures, the material properties of the gate oxide degrades. FN tunneling and high temperatures cause gate oxide to degrade and lose gate control. The second failure type is Aluminum melting. At high temperatures (>660 °C), Al starts to melt, diffuse into SiC, and penetrate the p-well of SiC, leading to drain-to-source shorting. The last failure type is related to thermally generated carriers. Although many research groups report thermal generated failure [1–3], it is hard to accept that thermal generated failure of SiC MOSFETs occurs at temperatures ~1600 °C since Al starts to melt at approximately 660 °C.

In order to explain the thermal generated failure, the importance of increasing temperature rate is introduced by [1]. In failure mechanism 1 and 2, a device does not immediately fail when reaching critical temperatures of material degradation, but will eventually be destroyed after a certain degradation time passes. In other words, failure mechanism 1 and 2 occur after significant degradation of device materials (gate oxide and Al source metal) takes place. These failure mechanisms appear when the low drain voltage is applied.

On the other hand, when junction temperature rapidly increases to the critical temperature of the thermal generation carrier (~1600 °C) and degradation time is short, failure mechanism 3 will occur first before failure mechanisms 1 and 2. Moreover, as surface temperature ($T_{\text{Surface}}$) is much lower than junction temperature ($T_{\text{Junction}}$), thermally generated current can be generated in SiC MOSFETs. Generally, the last mechanism occurs when a high drain voltage is applied. However, by the time of the thermally generated current, the other materials, such as gate oxide and Al source metal, are also mostly degraded, resulting in combined failure mechanisms during the
short-circuit condition. In this paper, we will focus on the gate failure mechanism using the developed Non-Isothermal simulation.

### 5.3. NON-IsoTHERMAL DEVICE SIMULATION

Using Sentaurus 2-D TCAD, Non-Isothermal simulations were conducted to investigate the influence of thin gate oxide and narrow JFET region on drain current and maximum junction temperature during the SC event. Sentaurus material library parameter sets related to SiC for Non-
Isothermal simulations are lacking in previous literature. Therefore, as part of the paper’s effort, thermal-related simulation models, such as thermal conductivity, mobility, interface trap, gate tunneling, and SRH lifetime, were established and optimized (Table 5.1 for summary) [7–12]. The temperature dependence of heat capacity and thermal conductivity for 4H-SiC can be given as

$$C_V = 4.10 \times 10^{-9}T^3 - 1.22 \times 10^{-5}T^2 + 1.29 \times 10^{-2}T - 0.685 \ [7] \quad (1)$$

$$K = (0.00105 \cdot T - 0.03)^{-1} \ [8] \quad (2)$$

The bulk mobility and channel mobility can be given as

$$\mu = \frac{\mu_{\text{max}}(T/300)^{-a}}{1 + [(N_D + N_A)/N_{\text{ref}}]^\gamma} \ [9-11] \quad (3)$$

, with parameters for electron and hole given in Table 5.1. In addition, for threshold voltage, $V_{th}$, both acceptor type traps, $Q_A$, and positive fixed charge, $Q_F$, is included at SiO$_2$/SiC interface, which is $Q_A = 1.5 \times 10^{12} \text{ cm}^{-2}$, $E_c-E = 0.18 \text{eV}$, and $Q_F = 2 \times 10^{11} \text{ cm}^{-2}$ [9], [11]. Finally, Shockley-Read-Hall (SRH) lifetime can be given as

$$\tau_{n,p} = \frac{\tau_{\text{max}}(T/300)^\beta}{1 + [(N_D + N_A)/N_{\text{ref}}]^\gamma} \ [12] \quad (4)$$

, with parameters for electron and hole given in Table 5.1.

Fig. 5.1 shows a cross section of a conventional accumulation-channel SiC MOSFET with $t_{ox}$ of 50 nm, half JFET width ($W_{JFET}$) of 0.7 µm, and a diagram of the equivalent circuit for producing a SC event [13]. For a 1.2kV SiC MOSFET, a drift layer doping concentration of $8 \times 10^{15} \text{ cm}^{-3}$ and thickness of 10 µm are designed in simulation. In order to increase channel mobility, an accumulation mode channel is used. The SC simulation with conventional structure uses an $R_g$ of 3 Ω, $V_{ds}$ of 800 V, and $V_{gs}$ of 20 V. Fig. 5.2 shows simulated results of drain current, maximum
Fig. 5.1. (a) Cross section of simulated conventional MOSFET and (b) diagram of the equivalent circuit for the short-circuit.

Fig. 5.2. Simulated drain current and maximum junction temperature in SiC.
Fig. 5.3. Applied gate voltage from +20 to -10 V during SC events.

junction temperatures (T_{j,max}), and gate voltage during the short-circuit event for the conventional MOSFET structure. At the start of the SC condition, maximum drain current occurs, resulting in high junction temperatures and a reduction of V_{th}. Next, drain current decreases due to the decrease in electron mobility at high temperatures, despite the lowering of V_{th}. High temperatures also contribute to the increase in the gate leakage current due to Fowler-Nordheim (FN) tunneling, which causes gate voltage to decrease, as shown in Fig. 5.3. This is because the gate leakage current leads to the voltage drop in the gate resistor (R_g). Decreased gate voltage can represent the degradation of the gate oxide. In this paper, a short-circuit failure event at time \( t_{sc} \) is defined when a change in gate voltage, \( \Delta V_{gs} \), of 1 V occurs.

5.4. THIN GATE OXIDE

Fig. 5.4 shows output characteristics with different gate oxide thicknesses. In order to obtain the same \( R_{on,sp} \) and \( V_{th} \), different gate voltages and additional p-well implants in the channel region
Fig. 5.4. Simulated output characteristics with different gate oxides.

Fig. 5.5. Electric field under the forward blocking mode at 1600 V for gate oxide thickness of 20 nm and 50 nm.
are applied. Although the specific on-resistance of thin gate oxide is the same as that of the thick gate oxide, saturation current decreases with thinner gate oxides and reduced gate voltage, as shown in Fig. 5.4. However, the maximum electric field in the gate oxide at the middle of JFET region increases under the forward-blocking mode, as shown in Fig. 5.5.

Fig. 5.6 shows simulated results of drain current, maximum junction temperature, and gate
Fig. 5.8. Energy band diagrams of 4H-SiC MOS devices with different $t_{\text{ox}}$ and gate voltage at 300, 1000, and 1500 K.

Fig. 5.9. (a) Short-circuit time and electric field in gate oxide and (b) delta $V_{gs}$ and electric field in gate oxide.

voltage during the short-circuit event for MOSFET with different gate oxide thicknesses. During the SC event, as mentioned in Fig. 5.6, thin gate oxide has lower saturation current, enabling lower maximum junction temperature in SiC when compared with thicker oxide. Due to high junction temperature, more thermal generated current occurs in MOSFETs with thicker gate oxide. Moreover, these lower junction temperatures reduce Fowler-Nordheim tunneling, resulting in the low gate leakage current during the short-circuit event, as shown in Fig. 5.7. Fig. 5.8 shows energy band diagrams of 4H-SiC MOSFET with different gate oxide thicknesses and gate voltage at 300, 1000, and 1500 K using online band diagram program [14]. At 1500 K, thin gate oxide with $V_{gs}=10$
V has a higher, thicker barrier between SiC and SiO₂ at high temperatures.

Fig. 5.9 shows short-circuit time (t_{sc}) and delta V_{gs} (\Delta V_{gs}), and electric field in gate oxide as a function of gate oxide thickness. Short-circuit time increases for t_{ox}=20 nm when compared with thicker oxides, as shown in Fig. 5.7 and Fig. 5.9. This is due to lower junction temperature, contributing to low gate leakage and low gate voltage, resulting in a higher, thicker barrier between SiC and SiO₂ at high temperatures. On the other hand, thinner gate oxides cause increased gate-to-source capacitance (C_{gs}) producing lower dV_{gs}/dt, which limits the reduction in saturation current during the SC event [5]. As a result, thin gate oxides provide low saturation currents only near the start of the short-circuit event, which offers moderate t_{sc} improvement.

5.5. NARROW JFET REGION

Fig. 5.10 (a) shows specific on-resistance as a function of JFET width with different JFET doping concentrations and (b) output characteristics with different JFET widths. In order to achieve reduced saturation current and thereby an increase in short-circuit withstanding time, JFET width is reduced. Concurrently, it is necessary to increase JFET doping concentration to lower specific on-resistance to compensate for reduced JFET width, as shown in Fig. 5.10.

Fig. 5.11 (a) shows simulated results of drain current, maximum junction temperature, and gate voltage during the short-circuit event for MOSFET with different JFET widths. During the short-circuit capability, MOSFETs with narrow JFET width suppressed maximum saturation current, resulting in the reduction in maximum junction temperatures. Due to lower junction temperature, narrow JFET width avoids thermally generated current. Furthermore, in the same manner as the thin gate oxide, low temperatures lead to reduced FN tunneling, resulting in a low gate leakage current. However, unlike reduced gate oxide, narrow JFET width has high dV_{gs}/dt,
Fig. 5.10. (a) $R_{on,sp}$ as a function of JFET width with different JFET doping concentrations and (b) output characteristics with different JFET widths.

Fig. 5.11. (a) Simulated drain current and maximum junction temperature in SiC and (b) gate voltage.

contributing to the large reduction in saturation current during the SC event. As a result, maximum junction temperature decreases (Fig. 5.11 (a)), contributing to the decrease in $\Delta V_{gs}$ (Fig. 5.11 (b)), thanks to the suppression of FN tunneling. Temperature distribution in SiC with different JFET widths at the short-circuit time of 5 µs is shown in Fig. 5.12. The MOSFET with a JFET width of 0.3 µm has largely lower junction and surface temperatures when compared with that with a JFET width of 0.7 µm. The temperature rises beneath gate oxide, especially near the n+ source, is significantly lower with narrow JFET width, allowing the reduction in FN tunneling.
Fig. 5.12. Temperature distribution of half JFET width = 0.3 and 0.7 µm.

Fig. 5.13. Summary of simulation results for \( t_{sc} \) and \( R_{on,sp} \).

Table 5.2. Summary of simulated results.

<table>
<thead>
<tr>
<th></th>
<th>Tox (nm)</th>
<th>( W_{JFET} ) (µm)</th>
<th>JFET doping (cm(^{-3}))</th>
<th>( V_{gs} ) (V)</th>
<th>( R_{on,sp} ) (mΩ-cm(^2))</th>
<th>( BV ) (V)</th>
<th>( E_{ox} ) (MV/cm)</th>
<th>( t_{sc} ) (µs)</th>
</tr>
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<tr>
<td>1</td>
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<td>0.7</td>
<td>( 3 \times 10^{15} )</td>
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<td>2.71</td>
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<td>3.39</td>
<td>8.5</td>
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<td>( 3 \times 10^{15} )</td>
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<td>1662</td>
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<tr>
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<td>( 3 \times 10^{15} )</td>
<td>16.6</td>
<td>2.71</td>
<td>1659</td>
<td>3.15</td>
<td>6.8</td>
</tr>
<tr>
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<td>20</td>
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<td>20</td>
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<td>1677</td>
<td>2.3</td>
<td>8.2</td>
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<tr>
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<td>1690</td>
<td>1.47</td>
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</table>

Fig. 5.13 and Table 5.2 summarize the simulated results. When using reduced JFET width, short-circuit capability is improved from 6.8 to 13.7 µs, as shown in Fig. 5.11 (b) and Fig. 5.13. Not only static (lower \( R_{on,sp} \), lower maximum electric field in gate oxide, and higher breakdown voltage) and dynamic (high \( dV_{gs}/dt \)) performance, but also SC capability (longer \( t_{sc} \), lower \( I_{sat} \),...
reduced $T_{j,max}$) is improved when using SiC MOFSET with narrow JFET regions with increased JFET doping concentration.

5.6. CONCLUSION

Non-Isothermal simulation for SC capability is performed to examine different types of SiC MOSFET structures. To obtain exact simulation results, thermal-related simulation models are developed and optimized. Thin gate oxide slightly increases short-circuit time while maintaining specific on-resistance due to reduced saturation current. However, the reduced gate oxide approach has drawbacks due to the increase in input capacitance, resulting in slow $dV_{gs}/dt$. Moreover, the MOSFET with thin gate oxide has a higher electric field in the gate oxide when compared to MOSFET with thicker gate oxide. Ultimately, it is demonstrated in Non-Isothermal simulation that reduced JFET width with increased JFET doping concentration largely enhances both static performances and short-circuit capability of SiC MOSFETs.

5.7. ACKNOWLEDGMENT

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Chapter 6

Analysis for Cell Topologies of 1.2 kV 4H-SiC Planar MOSFETs

6.1. INTRODUCTION

1.2 kV SiC MOSFETs are becoming more widely used in power electronics across various applications due to superior characteristics over conventionally employed Si IGBTs of similar rating. Depending on the specific application, the importance of various requirements, from a power semiconductor device perspective, is different. For example, low specific on-resistance is preferable to reduce conduction losses in electric vehicles (EV) [1]. High frequency applications need fast switching characteristics [2] to minimize switching losses. Aerospace and industrial applications require highly reliable and rugged devices [3]. In regards to the device architecture and process, many groups have been developing methods to improve conduction behavior [4], dynamic characteristics [5], and ruggedness [6]. However, detailed research regarding the layout approach, such as topology investigation of 1.2 kV 4H-SiC MOSFETs, is lacking; despite the specific attributes of a given power MOSFET topology fundamentally factoring into how the device performs. Consequently, it is of extreme interest to investigate SiC power MOSFET layout topology variations to understand which topologies are best suited for which applications.

In this paper, different layout topologies (linear and hexagonal) and different design variations (with and without the bridge of P-well) are compared using the same mask set and process baseline to then propose a suitable SiC power MOSFET type for each application of interest. The comparison between different devices was performed in terms of the statics, dynamic switching, and short-circuit characteristics.
Fig. 6.1. Layout of (a) Linear MOSFET, (b) HEXFET, (c) B- (Bridged) HEXFET, cross-sectional view of (d) A-A’, (e) B-B’, (f) C-C’.

6.2. DEVICE DESIGN

Fig. 6.1 shows layout and cross-sectional views of the 1.2 kV SiC MOSFETs with different topologies, each having a channel length (L_{ch}) of 0.4 μm and half JFET width (1/2W_{JFET}) of 0.7 μm. Accumulation-mode channel MOSFETs were designed to obtain higher channel mobility. In order to minimize JFET resistance, JFET implantation with a current spreading layer (CSL) was adopted in the fabricated MOSFETs. P+ source is placed in the orthogonal direction to reduce the cell pitch in MOSFET with the linear topology, as shown in Fig. 6.1 (a). Fig. 6.1 (d) and (e) pertain to the MOSFET with orthogonal P+ sources and show the cross-sectional views of portions that include N+ source contact and P+ source contact, respectively. However, the cell pitch of
MOSFETs with hexagonal topology increases due to the inclusion of a P+ source, as shown in Fig. 6.1 (b), (c), and (f). Although hexagonal topology has a wider cell pitch, the high conduction behavior can be maintained due to the higher channel density. A p-well bridge structure was added to protect the corner of the hexagonal p-well from high electric-field concentrations (B-HEXFET, Fig. 6.1 (c)).

6.3. DEVICE FABRICATION TECHNOLOGY

The devices were fabricated by Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, using the same base process line described in [7]. A 10 µm thick drift layer with N-type doping concentration of $8 \times 10^{15}$ cm$^{-3}$ on 6-inch, N+ 4H-SiC substrate was used for the fabrication of 1.2 kV MOSFETs. Aluminum and Nitrogen ion implants were used to form P-well/P+ source/JTE, and JFET region/N+ source, respectively. After all implantation steps were done, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed by a combination of ultrathin (2 nm) thermal oxide and 48 nm of deposited oxide, followed by a post oxidation anneal (POA) in N$_2$O ambient. The N-type polysilicon was deposited and patterned for the formation of the gate. After, undoped silicon glass (USG) was deposited as interlayer dielectric (ILD), then patterned and etched to make ohmic contact regions. Nickel (Ni) was deposited on the frontside, followed by an RTA for the silicidation process. Next, unsilicided Ni metals were removed and annealed by RTA at 965 °C for 2 minutes. The backside was then deposited with Ni, followed by the same RTA process. A 4 µm thick Ti/TiN/Al stack was deposited for the source and gate metal. Silicon nitride and polyimide were used for passivation. Finally, a solderable metal stack was deposited on the backside.
6.4. Results

6.4.1. Static Characteristics

Fig. 6.2 (a) shows the output characteristics of 1200 V/30 A HEXFET. The measurement was conducted at gate biases of 5 to 20 V with 5 V steps. The high conduction behaviors were achieved thanks to expertly optimized cell structure and process. The JFET region was optimized using the enhanced JFET doping with the current spreading layer (CSL). Moreover, by using the accumulation mode channel, the channel resistance was minimized. Fig. 6.2 (b) compares the output characteristics of the different topologies (note: substrate thinning process was not employed). $R_{on,sp}$ was extracted at $V_{gs}$ of 20 V and $V_{ds}$ of 1 V. As noticed, HEXFET offers the lowest $R_{on,sp}$ due to higher channel density as summarized in Table 6.1. Since the P-well bridge reduces the current path in the JFET area, $R_{on,sp}$ is higher in the case of B-HEXFET.

Transfer characteristics and transconductance are shown in Fig. 6.3 (a). Transfer characteristics were measured at $V_{ds}$ of 0.1 V. Regardless of topologies and designs, threshold voltages ($V_{th}$) are identical (2.3 V), but hexagonal topology provides low maximum transconductance ($G_m$) because the channel conductance for hexagonal structures is lower when compared with linear MOSFETs at the same gate voltage. Especially, B-HEXFET has the lowest channel conductance, resulting in the lowest $G_m$.

Fig. 6.3 (b) shows the blocking characteristics of the fabricated devices. In order to look into the cause of the leakage current, different gate voltages were applied under the blocking mode of operation. At $V_{gs}$ of -5 V, regardless of the split, high breakdown voltages with low leakage currents were achieved thanks to the efficient edge termination technique (Hybrid-JTE). When the negative gate voltage is applied, the channel is closed, which contributes to the formation of high
Fig. 6.2. Output characteristics of (a) HEXFET and (b) all devices. \( R_{\text{on,sp}} \) was extracted at \( V_{gs} = 20 \) V and \( V_{ds} = 1 \) V.

channel potential. The maintained channel potential under high drain voltage suppresses the leakage currents for all devices, especially the linear MOSFET. On the other hand, the leakage current increases at \( V_{gs} = 0 \) V. In other words, leakage current stems from the channel under blocking mode at \( V_{gs} = 0 \) V. HEXFET and B-HEXFET provide high breakdown voltage at \( V_{gs} = 0 \) V with low leakage until the breakdown, where the channel is effectively shielded by the
Fig. 6.3. (a) Transfer characteristics, and (b) blocking behaviors of fabricated devices. $V_{th}$ was extracted at $V_{ds}=0.1$ V and $I_{ds}=1$ mA.

hexagonal topology of P-well. Although hexagonal topology has higher channel density, the increased channel potential due to the surrounding P-well results in the reduction of the leakage current from the channel. Especially, B-HEXFET has a lower leakage current because the bridge of the P-well improves the shielding effect.
6.4.2. Switching Characteristics

Fig. 6.4, Fig. 6.5, and Fig. 6.6 show the measured switching waveforms of turn-on and turn-off for linear MOSFET, HEXFET, and B-HEXFET, respectively. A double pulse test was used to evaluate the switching characteristics of the devices. A DC supply voltage of 800 V was applied. The off/on gate voltage is -4/20 V, respectively, with $R_g$ of 20 $\Omega$ used for the switching test. The switching energies for turn-on and turn-off are calculated at 10% $V_{gs}$ to 10% $V_{ds}$ and 90% $V_{gs}$ to 90% $V_{ds}$, respectively. The switching results for all devices are summarized in Table 6.1. Linear MOSFET has the fastest switching behaviors for turn-on and turn-off. This is because linear MOSFET has low gate-drain capacitance ($C_{rss}$) [8] and high transconductance. HEXFET has high $E_{sw(off)}$ when compared with B-HEXFET in spite of low $R_{on,sp}$. The removal of the P-well bridge causes an increase in the JFET region, resulting in high $C_{rss}$.

Fig. 6.4. Switching waveforms of linear MOSFET: (a) turn-on (b) turn-off at $V_{gs}$=-4/20 V ($R_g$ = 20 $\Omega$) and $V_{ds}$=800 V. Switching speeds: $t_{sw(on)}$ = 62.4 ns, $t_{sw(off)}$ = 74.7 ns, Switching $dv/dt$: switching on= 21.1 kV/μs, switching off= 24.3 kV/μs, Switching losses ($V_{dc}$ = 800 V, $I_{ds}$= 18A): $E_{sw(on)}$ = 333 $\mu$J, $E_{sw(off)}$ = 206 $\mu$J.
Fig. 6.5. Switching waveforms of HEXFET: (a) turn-on (b) turn-off at $V_{gs}=-4/20$ V ($R_g=20$ Ω) and $V_{ds}=800$ V. **Switching speeds:** $t_{sw(on)}=63.2$ ns, $t_{sw(off)}=78.6$ ns, **Switching $dv/dt$:** switching on $=17.1$ kV/μs, switching off $=19.0$ kV/μs, **Switching losses** ($V_{dc}=800$ V, $I_{ds}=18$A): $E_{sw(on)}=378$ μJ, $E_{sw(off)}=276$ μJ.

Fig. 6.6. Switching waveforms of B-HEXFET: (a) turn-on (b) turn-off at $V_{gs}=-4/20$ V ($R_g=20$ Ω) and $V_{ds}=800$ V. **Switching speeds:** $t_{sw(on)}=58.8$ ns, $t_{sw(off)}=63.5$ ns, **Switching $dv/dt$:** switching on $=17.2$ kV/μs, switching off $=25.0$ kV/μs, **Switching losses** ($V_{dc}=800$ V, $I_{ds}=18$A): $E_{sw(on)}=401$ μJ, $E_{sw(off)}=258$ μJ.

6.4.3. Short-circuit Characteristics

Fig. 6.7 shows short-circuit (SC) waveforms of B-HEXFET. The SC condition is $R_g$ of 20 Ω, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V. At the beginning of the SC test, maximum drain current occurs, contributing to the increase of junction temperature. Next, the drain current starts decreasing because of the reduction in electron mobility at high temperatures.

Fig. 6.8 (a) shows the drain current density of B-HEXFET with different gate pulse widths.
Fig. 6.7. Short-circuit robustness waveforms of B-HEXFET under $V_{gs}=20$ V and $V_{ds}=800$ V.

Fig. 6.8. (a) Drain current density of B-HEXFET with different gate pulse widths under short-circuit condition at $V_{gs}=20$ V and $V_{ds}=800$ V. (b) Drain current density of all devices when the device is failure under the short-circuit condition. For linear MOSFET, HEXFET, and B-HEXFET, SCWT (maximum current density) of 1.3 $\mu$s (7822 A/cm$^2$), 1.0 $\mu$s (8487 A/cm$^2$), and 1.4 $\mu$s (6830 A/cm$^2$) was achieved.

In order to obtain short-circuit withstand time (SCWT, $t_{sc}$), the gate pulse width increases by 0.1 $\mu$s until the devices failed. SCWT of 1.4 $\mu$s was achieved in B-HEXFET. Although the device endured a gate pulse width of 1.5 $\mu$s, B-HEXFET failed after the completion of the SC condition. This is due to the junction temperature decreasing much more slowly in the device than the SC
drain current. Therefore, the DUT was continuously exposed to detrimental high temperatures, ultimately resulting in the degradation and failure of the device.

Fig. 6.8 (b) compares the drain current density of all devices when the device is failure under SC event. The lowest maximum current density ($J_{\text{peak}}$), contributing to the reduction in the junction temperature was accomplished in B-HEXFET. A low $J_{\text{peak}}$ results in the increase of $t_{\text{sc}}$, as the bridge of the P-well in the JFET region suppresses the current during SC conditions. Although HEXFET provides better shielding effects under blocking characteristics, the highest maximum drain current density occurs under SC event, resulting in the shortest SCWT. This is due to the significantly reduced $R_{\text{on,sp}}$.

Table 6.1 summarizes design information and experimental results for linear MOSFET, HEXFET, and B-HEXFET. In order to compare the different topologies and designs, the cell pitch and the portion of the cell were examined. The typical static characteristics, switching test, and short-circuit ruggedness were investigated to fairly compare the different layouts. HEXFET offers the lowest $R_{\text{on,sp}}$ with low leakage current, providing high breakdown voltage, which can be used in power electronics that require high-efficiency performance. In high-frequency applications, linear MOSFET can be utilized due to the low switching losses for both turn-on and turn-off. For critical applications that require extreme ruggedness, hexagonal topology with the bridge of P-well is favorable, since B-HEXFET provides a better shielding effect, resulting in improved reliability and robustness.
Table 6.1. Summary of design information and experimental results.

<table>
<thead>
<tr>
<th></th>
<th>MOSFET</th>
<th>HEXFET</th>
<th>B-HEXFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell pitch (μm)</td>
<td>4.4</td>
<td>5.9</td>
<td>5.9</td>
</tr>
<tr>
<td>Channel area (%)</td>
<td>32</td>
<td>35</td>
<td>29</td>
</tr>
<tr>
<td>$R_{on,sp}$ [mΩ·cm$^2$] @ V$<em>{gs}$=20 V and V$</em>{ds}$=1 V</td>
<td>3.34</td>
<td>2.83</td>
<td>3.42</td>
</tr>
<tr>
<td>$V_{th}$ [V] @ I$_{ds}$=1 mA</td>
<td>2.3</td>
<td>2.3</td>
<td>2.3</td>
</tr>
<tr>
<td>$G_{m(max)}$ [S]</td>
<td>0.14</td>
<td>0.134</td>
<td>0.114</td>
</tr>
<tr>
<td>BV [V] @ V$_{gs}$=0 V</td>
<td>1452</td>
<td>1554</td>
<td>1586</td>
</tr>
<tr>
<td>Leakage current [μA] @ V$<em>{gs}$=0V, V$</em>{ds}$=1200 V</td>
<td>9</td>
<td>0.1</td>
<td>0.04</td>
</tr>
<tr>
<td>$t_{sw(on)}$ [μs] @ V$<em>{gs}$=-4/20 V and V$</em>{ds}$=800 V</td>
<td>62.4</td>
<td>63.2</td>
<td>58.8</td>
</tr>
<tr>
<td>$t_{sw(off)}$ [μs] @ V$<em>{gs}$=-4/20 V and V$</em>{ds}$=800 V</td>
<td>74.7</td>
<td>78.6</td>
<td>63.5</td>
</tr>
<tr>
<td>Switching dv/dt (on) [kV/μs]</td>
<td>21.1</td>
<td>17.1</td>
<td>17.2</td>
</tr>
<tr>
<td>Switching dv/dt (off) [kV/μs]</td>
<td>24.3</td>
<td>19.0</td>
<td>25.0</td>
</tr>
<tr>
<td>$E_{sw(on)}$ [μJ] @ V$<em>{gs}$=-4/20 V and V$</em>{ds}$=800 V</td>
<td>333</td>
<td>378</td>
<td>401</td>
</tr>
<tr>
<td>$E_{sw(off)}$ [μJ] @ V$<em>{gs}$=-4/20 V and V$</em>{ds}$=800 V</td>
<td>206</td>
<td>276</td>
<td>258</td>
</tr>
<tr>
<td>$J_{peak}$ (A/cm$^2$) @ V$<em>{gs}$=20 V and V$</em>{ds}$=800 V</td>
<td>7822</td>
<td>8487</td>
<td>6830</td>
</tr>
<tr>
<td>$t_{sc}$ (μs) @ V$<em>{gs}$=20 V and V$</em>{ds}$=800 V</td>
<td>1.3</td>
<td>1</td>
<td>1.4</td>
</tr>
</tbody>
</table>

6.5. CONCLUSION

1.2 kV 4H-SiC MOSFETs with different layout topologies (linear and hexagonal) and different design variations (with and without the bridge of P-well) were investigated to study their effect on the static conduction, dynamic switching, and short-circuit characteristics. HEXFET provides the lowest $R_{on,sp}$ with high breakdown voltage due to the high channel area. Linear MOSFET has a fast switching speed because of the low $C_{rss}$ and high $G_m$. A p-well bridge allows...
B-HEXFET to be more reliable and rugged thanks to the shielding effect. Experimental measurements demonstrate which topologies are best suited for which power electronics applications.

6.6. ACKNOWLEDGMENT

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6.7. REFERENCES


Chapter 7

Optimization of 1.2 kV 4H-SiC MOSFETs with Channel Diodes

7.1. INTRODUCTION

SiC Schottky Barrier Diodes (SBDs) have been used in parallel with SiC MOSFETs as a freewheeling diode in power converter applications because the inherent PN body diode of the MOSFET has relatively high forward voltage drop, the considerable reverse recovery current, and suffers from the expansion of stacking faults over the lifetime of the device [1]. However, an additional external diode requires extra space within a multi-chip package or power module, and adds undesirable parasitic inductance to the power loop during commutation events of the power converter. Alternatively, when the unipolar diode structure is integrated within the MOSFET, a significant reduction in wafer area is achieved by sharing active and edge termination areas. Monolithic integration of Schottky or JBS diode in a SiC MOSFET structure (JBSFET) and SiC MOSFET integrating the unipolar internal inverse channel diode were reported earlier [2–5], respectively. However, JBSFET from [2] has higher specific on-resistance due to the larger cell pitch from the portion of the JBS diode when compared with standalone MOSFET. For [5], the fabrication of the proposed MOSFET requires a very thin and heavily doped epitaxial regrowth process, which may result in a complicated process.

In this paper, eliminating the regrowth process, 4H-SiC MOSFETs with inherent unipolar diode are proposed by controlling channel design parameters: channel doping, channel length, and gate oxide. MOSFETs with various channel doping concentrations, channel lengths, and gate oxides were successfully fabricated and investigated. In order to further clarify the effect of
channel potential, Sentaurus 2D TCAD was implemented and utilized. In addition, the reverse recovery characteristics and switching characteristics are discussed.

### 7.2. Device Concept

Fig. 7.1 shows the cross-sectional SEM image of the 1.2 kV MOSFET with accumulation mode channel [6]. The proposed accumulation mode channel needs to be optimized to satisfy low
Fig. 7.2. (a) Designed implant profiles for JFET and P-well implantation using SPROCESS. (b) Net doping profile.

on-resistance, unipolar operation in the 3rd quadrant (3Q) mode, and low leakage in the blocking mode, as shown in Table 7.1. Fig. 7.2 (a) shows designed implant profiles for the JFET and P-well implantation using process simulation from Synopsys [7]. The net doping was calculated based on Fig. 7.2 (a), as shown in Fig. 7.2 (b). The accumulation mode channel was formed by only using JFET and P-well implants [6]. The doping and depth of the accumulation channel were determined by JFET implants.

The key aspect to consider for a MOSFET with a channel diode is the potential barrier in the channel region. Fig. 7.3 (a) and (b) show simulated electrostatic potential at the channel region under third quadrant conduction mode and forward blocking mode, respectively. When the potential barrier between the channel and JFET region is overcome by applying negative drain-source voltage ($V_{ds}$), current flows through the channel region even before the conduction of the PN body diode. The low potential barrier allows low knee voltage, providing the decrease of forward voltage drop during the 3Q operation. On the other hand, under the forward blocking mode, the potential barrier between the N+ source and channel region determines the blocking behaviors of MOSFETs. High positive drain voltage makes the potential barrier formed in the
Fig. 7.3. Simulated electrostatic potential at channel region of MOSFETs with accumulation mode channel under (a) third quadrant mode, (b) forward blocking mode, and (c) the cross-sectional view of simulated current density for accumulation mode channel MOSFETs at various drain voltages ($V_{gs}=0$ V).

channel low (in magnitude) and thin (in width). In order to suppress leakage current from the channel region, a high and wide channel potential is required. A specific channel design would result in a trade-off relationship between the third quadrant conduction mode and forward blocking...
mode. Therefore, an optimized channel design is required to provide both low knee voltage and high breakdown voltage with low leakage current. The channel potential is governed by various parameters such as channel doping, channel length, and gate oxide, which will be discussed in the next chapter.

Fig. 7.3 (c) shows cross-sectional views of simulated current density in the accumulation mode channel at various drain voltages. At $V_{ds}$ of 0 V, the channel is closed, resulting in insignificant current flow. At $V_{ds}$ of $\leq -1.0$ V, current starts flowing through the channel regions. As the $V_{ds}$ decreases, so too does the current density due to the channel region becoming fully open, providing high conduction behavior. The PN body diode also turns on at $V_{ds}$ of approximately -3.0 V and current flows through both the channel and body diode. Depending on the channel potential, the knee voltage of MOSFETs under third quadrant mode is altered, resulting in a change of the forward voltage drop. MOSFETs with low channel potential provide low knee voltage, which in turn enables then high current to flow through the channel region. Thus, MOSFETs with low knee voltage (attributed to a low channel potential) enable high reverse conduction currents to be commutated through the MOSFET before the operation of the PN body diode kicks in and begins to dominate reverse conduction behavior. However, extremely low knee voltage causes high leakage current in the forward blocking mode due to low channel potential. Therefore, it is important to optimize channel parameters to achieve low leakage current while maintaining low forward voltage drop during the 3rd quadrant behavior.

7.3. DEVICE FABRICATION TECHNOLOGY

The devices were fabricated at Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, USA [8], [9]. A 10 μm thick drift layer with N- epi doping concentration of about
8×10^{15} \text{cm}^{-3} \text{ on a 6-inch, N+ 4H-SiC substrate was used for the fabrication of 1.2 kV MOSFETs. Aluminum and Nitrogen ion implants were implemented to make P-well/P+ body/JTE, and JFET/N+ source, respectively. The average doping concentrations in the JFET region of 5×10^{16}, 7×10^{16}, and 9×10^{16} \text{cm}^{-3} \text{ were used to investigate the effect of the channel doping concentration on the operation of MOSFET with channel diode; the resultant effective channel doping are 3, 5, and 7×10^{16} \text{cm}^{-3}, \text{ respectively. After implantation steps, a 1650 °C 10-min activation anneal with a carbon cap was conducted. To investigate the impact of the gate oxide, MOSFETs with 3 different gate oxides were fabricated; 25 nm deposited- 50 nm deposited-, and 50 nm thermally grown- gate oxides. For the deposited gate oxide of 50 (25) nm, 2 nm thermal oxide was grown and then high temperature oxide (HTO) of 48 (23) nm was deposited. After the formation of the gate oxide, a post oxidation anneal (POA) in N\textsubscript{2}O ambient was implemented for high channel mobility. The N-type polysilicon was deposited and patterned for the formation of the gate. Afterwards, interlayer dielectric (ILD) was deposited, patterned, and etched to make ohmic contact regions. Nickel (Ni) was deposited on the front side, followed by RTA for the self-aligned silicidation process. Next, unsilicided Ni metals were removed and annealed by a 2-min RTA at 965 °C for the front side ohmic contact. Backside metal contact was also deposited using Ni, followed by the same RTA process. A 4 µm thick Ti/TiN/Al metal stack was deposited as the source and the gate metal. Silicon nitride and polyimide were used for passivation on the frontside. Finally, a solderable metal stack was deposited on the backside. No substrate thinning process was adopted.}
7.4. RESULTS AND DISCUSSIONS: OPTIMIZATION OF CHANNEL POTENTIAL

7.4.1. CHANNEL DOPING CONCENTRATION

Table 7.2 shows the description of the fabricated 4H-SiC MOSFETs to optimize the accumulation channel. Fig. 7.4 shows the cross-sectional SEM image of MOSFETs with a channel length ($L_{ch}$) of 0.5 µm and channel doping of $3 \times 10^{16}$ cm$^{-3}$. Fig. 7.5 shows the designed implant profile for different channel doping concentrations. Although channel depth is one of the important factors in channel potential, in this case, the effect of channel depth was included in that of the channel doping concentration.

Table 7.2. Device Description of the fabricated 4H-SiC MOSFETs.

<table>
<thead>
<tr>
<th></th>
<th>Gox thickness</th>
<th>Channel doping (#/cm$^3$)</th>
<th>$L_{ch}$ (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>Thermal (50nm)</td>
<td>$3 \times 10^{16}$</td>
<td>0.5</td>
</tr>
<tr>
<td>D2</td>
<td>Thermal (50nm)</td>
<td>$5 \times 10^{16}$</td>
<td>0.5</td>
</tr>
<tr>
<td>D3</td>
<td>Thermal (50nm)</td>
<td>$7 \times 10^{16}$</td>
<td>0.5</td>
</tr>
<tr>
<td>D4</td>
<td>Thermal (50nm)</td>
<td>$3 \times 10^{16}$</td>
<td>1.0</td>
</tr>
<tr>
<td>D5</td>
<td>Thermal (50nm)</td>
<td>$3 \times 10^{16}$</td>
<td>0.4</td>
</tr>
<tr>
<td>D6</td>
<td>Thermal (50nm)</td>
<td>$3 \times 10^{16}$</td>
<td>0.3</td>
</tr>
<tr>
<td>D7</td>
<td>Deposited (50nm)</td>
<td>$3 \times 10^{16}$</td>
<td>0.5</td>
</tr>
<tr>
<td>D8</td>
<td>Deposited (25nm)</td>
<td>$3 \times 10^{16}$</td>
<td>0.5</td>
</tr>
</tbody>
</table>

*Gox=gate oxide, $L_{ch}$=channel length.

Fig. 7.4. The cross-sectional SEM image of 1.2 kV accumulation channel mode MOSFETs with a channel length of 0.5 µm and channel doping of $3 \times 10^{16}$ cm$^{-3}$.
Fig. 7.5. Designed implant profiles for channel region and P-well for different channel doping using SPROCESS.

![Fig. 7.5. Designed implant profiles for channel region and P-well for different channel doping using SPROCESS.](image)

Fig. 7.6. Measured (a) output and (b) transfer characteristics of MOSFETs with different channel doping.

![Fig. 7.6. Measured (a) output and (b) transfer characteristics of MOSFETs with different channel doping.](image)

channel doping. In other words, the channel depth is determined by various doping concentrations with a fixed P-well profile.

Measured forward conduction behaviors of the fabricated 1.2 kV MOSFETs with different channel doping ($L_{ch}$ of 0.5 µm) are shown in Fig. 7.6 (a). MOSFETs were measured at gate-source biases of 0 to 20 V with 10 V steps. The increase in channel doping provides better conduction behaviors. In terms of channel doping of 3, 5, and $7 \times 10^{16}$ cm$^{-3}$, the resultant $R_{on,sp}$ is 4.54, 4, and 3.83 m$\Omega$-cm$^2$, respectively (specific on-resistance was extracted from output characteristics at $V_{gs}$...
Fig. 7.7. Measured (a) third quadrant behaviors and (b) forward blocking mode at V_{gs} of 0 V of MOSFETs various channel doping.

of 20 V and V_{ds} of 0.1 V). Increased JFET doping and thus channel doping reduces the channel resistance as well as the JFET resistance. Fig. 7.6 (b) shows the transfer characteristics of MOSFETs with different channel doping. For D1, D2, and D3, V_{th} is 2.5, 2.2, and 1.7 V, respectively (V_{th} was extracted at V_{ds} of 0.1 V and I_{ds} of 5 mA).

Measured third quadrant behaviors and forward blocking mode of MOSFETs with various channel doping are shown in Fig. 7.7 (a) and (b), respectively. L_{ch} of 0.5 µm was used to examine the impact of channel doping. Due to the accumulation mode channel, MOSFETs provide current conduction with a knee voltage of 1~1.5 V under third quadrant mode as shown in Fig. 7.7 (a); the criteria of usable unipolar channel diode current was defined at a power density of 500 W/cm²
[10], [11]. The high channel doping results in the reduction in the knee voltage and the forward voltage drop under third quadrant behaviors due to the decrease of channel potential. However, low channel potential results in high leakage current, contributing to low breakdown voltage, as shown in Fig. 7.7 (b). The criteria to determine whether the low leakage current or high leakage current is 1 µA at V_{ds} of 1200 V. Channel doping of 3×10^{16} cm^{-3} for L_{ch} of 0.5 µm provides high
breakdown voltages with low leakage current. Although channel doping of $5 \times 10^{16} \text{ cm}^{-3}$ has high leakage current, it allows blocking of $>1.2 \text{ kV}$. However, it is difficult for channel doping of $7 \times 10^{16} \text{ cm}^{-3}$ to be used in SiC MOSFETs with a 1.2 kV rating due to low breakdown voltage. It is discovered that the optimized channel doping allows MOSFETs to provide low knee voltage and high conduction behaviors under the third quadrant mode with high breakdown voltage.

In order to elucidate the decreasing slope of the current under the third quadrant after operating the PN body diode, Sentaurus 2D TCAD simulation was conducted. Fig. 7.8 (a) shows the simulated current density of MOSFETs with low and high P contact resistance at $V_{ds}$ of -1.5 V and -4.5 V, which are before and after operating the PN body diode, respectively. Fig. 7.8 (b)
Fig. 7.9. Simulated electrostatic potential at channel region of MOSFETs with various channel doping concentrations.

Fig. 7.10. (a) Measured output characteristics of MOSFETs with channel doping of $7 \times 10^{16}$ cm$^{-3}$ at different temperatures, (b) summary of experimental $R_{on,sp}$ at different temperatures, and measured third quadrant behaviors at (c) 100 °C, and (d) 175 °C.
shows the drain current density of MOSFETs with low and high P contact resistance. Before PN body diode operation, drain current density is identical regardless of P contact resistance. However, MOSFETs with low P contact resistance allow current density to be high after the PN body diode turns on.

Fig. 7.8 (c) shows the electron current density from N contact and P contact of MOSFETs with low and high P contact resistance. Not only is higher channel current density (i.e. current density from N contact) observed, but also higher body diode current density (i.e. current density from P contact) are achieved in MOSFETs with low P contact resistance when compared to MOSFETs with high P contact resistance, as shown in Fig. 7.8 (a) and (c). When the PN body diode turns on, the potential barrier in the channel is adjusted depending on P contact resistance, resulting in the change of electron conduction.

Fig. 7.9 shows simulated electrostatic potential near the surface, starting at the N+ source, proceeding through the channel, and ending in the JFET region of MOSFETs with various channel doping. It can be seen that the built-in potential between the channel and JFET decreases for the operation of the third quadrant when the channel doping increases. Moreover, the width of the potential barrier decreases with the increase of the channel doping. It clearly shows there is trade-off relationship between the third quadrant mode and blocking mode.

Fig. 7.10 (a) shows measured output characteristics of MOSFETs with channel doping of $7 \times 10^{16}$ cm$^{-3}$ at different temperatures. At room temperature, MOSFETs provide better conduction behaviors. This is because operation at high temperature results in a reduction in mobility, reducing the overall current conduction between drain and source. Fig. 7.10 (b) summarizes experimental $R_{on,sp}$ at different temperatures and channel doping concentrations. Regardless of channel doping, $R_{on,sp}$ increases with temperature. Fig. 7.10 (c) and (d) show measured third quadrant behaviors at
100 °C and 175 °C. The high temperature results in a decrease in knee voltage, but the forward voltage drop increases due to the reduction in mobility. Regardless of operating temperature, high channel doping provides better third quadrant behaviors.

### 7.4.2. Channel Length

Various L\textsubscript{ch} (1.0, 0.5, 0.4, and 0.3 µm) were designed to examine the impact of L\textsubscript{ch} on channel diode behavior. Due to the decrease of channel resistance, shorter L\textsubscript{ch} provides better conduction behaviors, resulting in lower specific on-resistance (R\textsubscript{on.sp}). For L\textsubscript{ch} of 0.3, 0.4, 0.5, and 1.0 µm, the resultant R\textsubscript{on.sp} is 4.02, 4.27, 4.54, and 6.54 mΩ-cm\textsuperscript{2}, respectively. Transfer characteristics of MOSFETs with different L\textsubscript{ch} are shown in Fig. 7.11 (a). For L\textsubscript{ch} of 0.3, 0.4, 0.5, and 1.0 µm, V\textsubscript{th} is 1.9, 2.2, 2.5, and 3.4 V, respectively (V\textsubscript{th} was extracted at V\textsubscript{ds} of 0.1 V and I\textsubscript{ds} of 5 mA).

Measured third quadrant behaviors of MOSFETs with different L\textsubscript{ch} are shown in Fig. 7.11 (b). At a power density of 500 W/cm\textsuperscript{2}, D1, D5, and D6 operate in the unipolar mode only using electron current. Shorter L\textsubscript{ch} provides low knee voltage, resulting in better conduction behaviors. This is because shorter L\textsubscript{ch} forms thinner and lower potential barrier in the channel region. In contrast to shorter L\textsubscript{ch}, D4 turns on the body diode from -2.7 V. It is observed that due to the unoptimized contact resistance of P+, the current slope is reduced when the operation of the body diode begins [12]; Fig. 7.11 (b).

Fig. 7.11 (c) shows the measured forward blocking mode of MOSFETs with various L\textsubscript{ch}. Shorter L\textsubscript{ch} (D5 and D6) has high leakage current and low breakdown voltage under blocking behaviors. Due to low channel potential, leakage current flows through the channel under high drain voltage, reaching a high leakage current before avalanche breakdown occurs. However, D1 and D4 provide high breakdown voltage with low leakage current, since L\textsubscript{ch} of > 0.5 µm forms a
sufficiently high channel potential that suppresses current conduction in the channel under high drain voltage. When the potential barrier in the channel supports high voltage, the breakdown voltage is then governed by the avalanche phenomenon at the end of the P-well region or edge termination, not leakage current.

Simulated electrostatic potential at the channel region of MOSFETs with different $L_{ch}$ is shown in Fig. 7.11 (d). In the same manner as channel doping, $L_{ch}$ shows trade-off relationship between barrier for the third quadrant and blocking mode. However, the potential between the N+ source and channel for blocking mode is affected by not only barrier height but also barrier
thickness. Long \(L_{ch}\) provides a thicker and higher potential barrier, providing a low leakage current under blocking mode. For the improvement of the trade-off relationship between the third quadrant and blocking mode, an appropriate channel length (e.g. \(D1\)) is required to operate MOSFETs that utilize the channel diode.

### 7.4.3. Gate Oxide

For the optimization of channel potential, MOSFETs with different thicknesses and types of gate oxide were fabricated. Different gate voltages were applied with different thicknesses of gate oxide; 50 nm (20 V) and 25 nm (12 V). Regardless of the gate oxide condition, conduction behaviors are almost identical. For \(D1, D7,\) and \(D8\), the resultant \(R_{on,sp}\) is 4.54, 4.73, and 4.57 m\(\Omega\)-cm\(^2\), respectively.

Transfer characteristics of MOSFETs with different gate oxides are shown in Fig. 7.12 (a). \(D8\) shows a reduced \(V_{th}\) because of the increased specific oxide capacitance \((C_{ox})\). Fig. 7.12 (b) shows a simulated \(V_{th}\) of MOSFETs with thermal gate oxide of 50 nm. It shows that \(V_{th}\) increases with gate oxide thickness. \(D1\) has a lower \(V_{th}\) when compared with \(D7\) which might be originated from a larger positive fixed charge. Fig. 7.12 (c) shows capacitance–voltage (C–V) characteristics of MOS capacitor with different gate oxides. It is shown that thermal gate oxide was more shifted in C-V measurement due to a larger positive fixed charge. The measured \(D_{it}\) for thermal and deposited gate oxide at \(E_c-E\) of 0.125 eV is approximately \(4 \times 10^{11}\) cm\(^2\)eV\(^{-1}\) and \(3 \times 10^{11}\) cm\(^2\)eV\(^{-1}\), respectively. Fig. 7.12 (d) shows measured input capacitances of MOSFETs with different gate oxides. Since input capacitances are largely affected by gate oxide thickness, a gate oxide thickness of 25 nm causes higher input capacitances when compared with MOSFETs with a gate oxide thickness of 50 nm.
Fig. 7.12. (a) Measured transfer characteristics of MOSFETs with different gate oxides, (b) simulated $V_{th}$ of MOSFETs with thermal gate oxide of 50nm, (c) measured capacitance-voltage (C-V) characteristics of MOS capacitor with different gate oxides, and (d) measured input capacitances of MOSFETs with different gate oxides.

Fig. 7.13. (a) Measured third quadrant behaviors and (b) forward blocking mode at $V_{gs}$ of 0 V of MOSFETs with $L_{ch}$ of 0.5 $\mu$m with different gate oxides.
Fig. 7.14. Simulated electrostatic potential at channel region of MOSFETs with (a) different gate oxide thickness, (b) different fixed charges in the gate oxide.

Fig. 7.13 (a) shows measured third quadrant behaviors of the fabricated 4H-SiC MOSFETs with different gate oxides. Different gate oxides provide different third quadrant behaviors, when accounting for the same channel doping and $L_{ch}$ conditions across MOSFETs. The difference in third quadrant conduction behavior originates from the potential barrier in the channel region. D1 has low knee voltage due to a larger fixed charge, resulting in a decrease in the channel potential. Although different gate oxides produce different knee voltages under third quadrant behaviors, blocking behavior remains identical, as shown in Fig. 7.13 (b). This is because despite D1 having the lowest knee voltage, these MOSFETs still maintain a high enough channel potential to block high drain voltage (>1.5 kV).

In order to clarify channel potential, Sentaurus 2D TCAD simulation was conducted. The thinner gate oxides result in lower channel potential, as shown in Fig. 7.14 (a). However, in contrast to channel length and doping variations, thinner gate oxide maintains the width of the potential barrier. As a result, the reduced thickness of gate oxide can improve the trade-off relationship between 3Q conduction and blocking behaviors. Moreover, the fixed charge in the gate oxide determines the change in the channel potential, as shown in Fig. 7.14 (b). A larger fixed
Fig. 7.15. Summary of the simulated channel potential for 3Q and blocking behaviors.

Fig. 7.16. Summary of the plot when potential barrier of BV divided by potential barrier of 3Q.

charge causes a low potential barrier. The fixed charge found within the gate oxide differs depending on the process or recipe used to form it. In this case, thermal gate oxide possesses a larger fixed charge when compared with deposited gate oxide, and as a result has a lower channel potential barrier, providing better conduction behavior under third quadrant mode.
Fig. 7.15 compares various approaches discussed earlier with respect to simulated channel potentials in the blocking mode and 3Q mode of operations. Fig. 7.16 plots the blocking potential barrier divided by the potential barrier for the 3Q operation. It is clearly discovered that the gate oxide thickness serves as an effective knob to control the blocking channel potential keeping smaller changes in the channel potential during 3Q operation. In other words, the change of gate oxide and channel length has a better trade-off relationship between 3Q and blocking behaviors. Moreover, the change of gate oxide thickness is the better way to improve the trade-off relationship as the width of the potential barrier is identical regardless of the thickness. However, it should be noted that a certain level of the blocking channel potential should be maintained to suppress the leakage current (The channel potential for BV of >~0.8 V is required to obtain high BV with a low leakage current; The channel potential value of 0.8 V is selected to ensure the leakage current does not exceed 100 μA at 1200 V).

7.5. RESULTS AND DISCUSSIONS: DYNAMIC CHARACTERISTICS

7.5.1. REVERSE RECOVERY CHARACTERISTICS

Fig. 7.17 (a) shows the simulated test circuit for the reverse recovery characteristics. MOSFET ‘B’ in Fig. 7.17 (a) is used as a freewheeling diode to evaluate the reverse recovery characteristics. Fig. 7.17 (b) shows the simulated reverse recovery characteristics of MOSFETs with different channel lengths. MOSFETs with short channel provide a small reverse recovery charge ($Q_{RR}$); For $L_{ch}$ of 0.3 μm, 0.5 μm, and 1.0 μm, $Q_{RR}$ of 0.97 μC/cm$^2$, 1.06 μC/cm$^2$, and 1.24 μC/cm$^2$ were extracted, respectively. MOSFETs with low knee voltage under third quadrant behaviors offer a small $Q_{RR}$. 
7.5.2. **Switching Characteristics**

Fig. 7.18 (a) and (b) show simulated switching waveforms of MOSFETs with different channel lengths in turn-on and turn-off, respectively. The MOSFETs with $L_{ch}$ of 0.3 μm have the fastest turn-on switching transient due to the largest transconductance [13]. For $L_{ch}$ of 0.3 μm, 0.5 μm, and 1.0 μm, energy loss for turn-on transient of 173 μJ, 298 μJ, and 335 μJ were calculated as

Fig. 7.17. (a) Test circuit for reverse recovery characteristics and (b) simulated reverse recovery characteristics of MOSFETs with different channel lengths.

Fig. 7.18. Simulated switching waveforms of MOSFETs with different channel lengths in (a) turn-on and (b) turn-off.
shown in Table 7.3. The switching energy for the turn-on transient is calculated at 10% $V_{gs}$ to 10% $V_{ds}$. The energy loss for the turn-off transient is almost identical regardless of channel length.

Fig. 7.19 shows simulated switching waveforms of MOSFETs with different gate oxides. The MOSFETs with gate oxide of 25 nm have a slow turn-on switching transient due to the large $C_{iss}$.

![Switching waveforms](image)

Fig. 7.19. Simulated switching waveforms of MOSFETs with different gate oxides in (a) turn-on and (b) turn-off.

Table 7.3. Summary of experimental and simulated results.

<table>
<thead>
<tr>
<th></th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>D5</th>
<th>D6</th>
<th>D7</th>
<th>D8</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{on,sp}$ [mΩ-cm$^2$]</td>
<td>4.54</td>
<td>4.00</td>
<td>3.83</td>
<td>6.54</td>
<td>4.27</td>
<td>4.02</td>
<td>4.73</td>
<td>4.57</td>
</tr>
<tr>
<td>$V_{th}$ [V]</td>
<td>2.5</td>
<td>2.2</td>
<td>1.7</td>
<td>3.4</td>
<td>2.2</td>
<td>1.9</td>
<td>3.5</td>
<td>1.9</td>
</tr>
<tr>
<td>$BV$ [kV]</td>
<td>1.56</td>
<td>1.42</td>
<td>1.24</td>
<td>1.58</td>
<td>1.53</td>
<td>0.91</td>
<td>1.56</td>
<td>1.56</td>
</tr>
<tr>
<td>$I_{leakage}$ [nA]</td>
<td>9.2</td>
<td>37</td>
<td>0.5mA</td>
<td>5.7 nA</td>
<td>19 μA</td>
<td>N/A</td>
<td>14.8 nA</td>
<td>8.4 nA</td>
</tr>
<tr>
<td>$-V_F$ [V]</td>
<td>3.51</td>
<td>3.21</td>
<td>2.92</td>
<td>5.9</td>
<td>3.02</td>
<td>2.78</td>
<td>4.26</td>
<td>3.74</td>
</tr>
<tr>
<td>$Q_{RR}$ [μC/cm$^2$]</td>
<td>1.06</td>
<td>-</td>
<td>-</td>
<td>1.24</td>
<td>-</td>
<td>0.97</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$E_{on}$ [μJ]</td>
<td>298</td>
<td>-</td>
<td>-</td>
<td>335</td>
<td>-</td>
<td>173</td>
<td>299</td>
<td>305</td>
</tr>
<tr>
<td>$E_{off}$ [μJ]</td>
<td>32.7</td>
<td>-</td>
<td>-</td>
<td>32.3</td>
<td>-</td>
<td>33.2</td>
<td>32.6</td>
<td>34.8</td>
</tr>
</tbody>
</table>

*R_{on,sp} was extracted at $V_{gs}$ of 20V (12V for 25nm) and $V_{ds}$ of 0.1V.

$V_{th}$ was extracted at $V_{ds}$ of 0.1V and $I_d$ of 5mA.

$BV$ was extracted at $I_d$ of 1mA.

$I_{leakage}$ was extracted at $V_{ds}$ of 1200V.

$V_F$ was extracted at $I_d$ of 10A.

$E_{on}$ was extracted at 10% $V_{gs}$ to 10% $V_{ds}$.

$E_{off}$ was extracted at 90% $V_{gs}$ to 90% $V_{ds}$.
However, energy loss for the turn-on transient was almost identical; For thermal 50 nm, deposited 50 nm, and deposited 25 nm, energy loss for turn-on transient of 298 μJ, 299 μJ, and 305 μJ were calculated, as shown in Table 7.3. This is because a small inrush current compensates for the slow switching speed in MOSFETs with 25 nm. The energy loss for the turn-off transient is also almost identical regardless of gate oxide; For thermal 50 nm, deposited 50 nm, and deposited 25 nm, 32.7 μJ, 32.6 μJ, and 34.8 μJ were extracted, as shown in Table 7.3.

Table 7.3 summarizes the experimental and simulated results. It turns out that short channel length improves switching characteristics as well as reverse recovery characteristics. However, MOSFETs with thin gate oxide cause increased input capacitance, resulting in a slow switching speed. The optimum way for channel diode is the optimization of channel length by reducing the channel length.

7.6. CONCLUSION

1.2 kV SiC MOSFETs achieving a low knee voltage, as well as low forward voltage drop, under the third quadrant mode of operation are proposed and experimentally demonstrated. This paper provides MOSFET designers with a more manageable fabrication process by removing the regrowth process. Also, the optimization of channel potential was investigated in terms of trade-off between blocking mode and third quadrant behaviors. The reduced L_{ch} or increased channel doping results in the reduction in channel potential, contributing to the decrease of knee voltage under the third quadrant mode. Moreover, shorter L_{ch} or increased channel doping provide low R_{on,sp} due to low channel resistance or JFET resistance. Too shorter L_{ch} and high channel doping result in low breakdown voltage due to high leakage current from the channel, but L_{ch} of 0.5 μm (channel doping of 3×10^{16} cm^{-3}) have high breakdown voltage with extremely low leakage current.
The effect of thickness and fixed charge of gate oxide for channel potential was also discussed. It is demonstrated thinner thickness and larger fixed charge provide better third quadrant behaviors due to the low channel potential. 1.2kV MOSFETs with channel diode are successfully fabricated using the optimization of channel doping, $L_{ch}$, and gate oxide. Moreover, the simulated reverse recovery characteristics and switching characteristics are discussed. MOSFETs with short channel lengths improve not only reverse recovery characteristics but also switching characteristics. Consequently, the optimized 4H-SiC MOSFETs with channel diode are promising and suitable power semiconductor devices for power electronics.

7.7. ACKNOWLEDGMENT

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7.8. REFERENCES


Chapter 8

Demonstration of 1.2 kV 4H-SiC MOSFETs with Superior Short-circuit characteristics

8.1. INTRODUCTION

SiC MOSFETs have been improved in regards to specific on-resistance (R_{on,sp}) and breakdown voltage (BV) with improvement in the gate oxide recipes [1] and edge termination efficiencies [2], respectively. However, 4H-SiC MOSFETs still elicit reliability and ruggedness concerns [3], [4]. Specifically, 1.2 kV 4H-SiC MOSFETs provide shorter short-circuit withstand time (SCWT) due to high electric fields at the PN junction within the MOSFET structure and higher current densities when compared to Si insulated gate bipolar transistors (IGBTs). Lower channel/JFET density [5], source doping reduction [6], and the use of lower gate bias [7], [8] have been proposed to enhance short-circuit (SC) ruggedness. However, increased SCWT using these approaches results in increased R_{on,sp}.

In this paper, a novel approach to improve the trade-off relationship between SCWT and R_{on,sp} is proposed using MOSFETs with a deep P-well structure utilizing channeling implantation. The concept of channeling implantation has been reported to form deep junctions using low implant energy [9-13]. In order to conduct the channeling implantation, a tilt angle of 4 degrees was adjusted to <0001> direction of 4H-SiC in 4H-SiC (0001) substrates with 4 ° off-cut towered <11-20> direction [10]. Extremely high energy is required to form deep junctions during conventional implantation (random implantation), where the thickness of the hard mask or crystal damage during random implants are problematic. On the other hand, channeling implants with low energy provide deep junctions without any additional nor complicated processes. Although the concept of
channeling implantation has been introduced earlier, the application and demonstration of channeling implantation in SiC MOSFETs have not been achieved. This paper reports the successful fabrication and demonstration of MOSFETs with deep P-well structures using channeling implantation.

8.2. DEVICE STRUCTURE AND FABRICATION TECHNOLOGY

Fig. 8.1 (a) and (b) show the cross-sectional view of the conventional and proposed MOSFETs, respectively. The same channel length of 0.5 μm was designed and the JFET region was optimized to minimize the JFET resistance. To form the deep P-well regions, room-temperature channeled implants were conducted at a tilt angle of 4 degrees with Al and P dopants at 350 keV and 960 keV, respectively. It is important to note that there are no additional photo mask processes to fabricate the proposed MOSFETs with deep P-well. In order to form the deep JFET and P-well, an additional channeling implant was conducted during each implantation. The channeling implant, which enables the formation of deep junctions using low implant energy, is
Fig. 8.2. Implant profiles for conventional and proposed P-wells based on SIMS and SPROCESS [14]. The proposed P-well is composed of conventional random implant as well as channeling implant. The channeling implant schedule was designed based on the SIMS profile.

vital to achieve improved SCWT in the proposed MOSFET structure. The implant profiles for the P-well of the conventional and proposed MOSFETs are shown in Fig. 8.2. The depth of channeling implants provides around 2.5 times deeper implant than that of the random implants using similar energy of Aluminum.

The MOSFETs were fabricated by SiCamore Semi, OR, U.S.A. A 10 μm thick drift layer with an N-type doping concentration of $8\times10^{15}$ cm$^{-3}$ on an N+ 4H-SiC substrate was used for the fabrication of the 1.2 kV MOSFETs. Two wafers were used to fabricate both the conventional and proposed MOSFETs for a fair comparison. For the conventional MOSFETs, random implants for Aluminum and Nitrogen were used to form the P-well/P+ source/JTE, and JFET/N+ source, respectively. In order to fabricate the proposed MOSFETs, additional channeling implants for Aluminum and Phosphorus during the P-well and JFET implants were conducted for the formation of the deep P-well and JFET regions, respectively. Since Nitrogen only provides a small channeling effect in SiC [12], Phosphorus was utilized for the formation of the deep JFET region.
Fig. 8.3. Typical output characteristics of conventional and proposed 1.2 kV MOSFETs. The measured threshold voltages ($V_{th}$) were extracted from transfer characteristics at a drain voltage of 1 V and drain current of 5 mA. $V_{th}$ for the conventional and proposed MOSFETs are 2.6 V and 2.7 V, respectively.

Fig. 8.4. Forward blocking characteristics of fabricated 1.2 kV MOSFETs.

At the conclusion of all the implantation steps, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed, followed by a post oxidation anneal (POA). N-type polysilicon was deposited and patterned for the formation of the gate. After interlayer dielectric (ILD) was deposited, the ILD was then patterned and etched to make ohmic contact regions. Nickel (Ni) was deposited on the frontside, followed by an RTA for the silicidation process.
process. Next, unsilicided Ni metals were removed and annealed by RTA. Ni was then deposited on the backside, followed by the same RTA process. The source and gate metal based on Al were deposited, patterned, and etched. For the passivation, Silicon nitride was deposited, patterned, and etched. Finally, a solderable metal stack was deposited on the backside.

8.3. EXPERIMENTAL RESULTS AND DISCUSSIONS

Fig. 8.3 shows measured output characteristics of the fabricated 1.2 kV–rated SiC MOSFETs. Under the application of a $V_{gs}$ of 20 V and a $V_{ds}$ of 1 V, the conventional and proposed MOSFETs have almost identical behaviors; $R_{on,sp}$ at $V_{gs}$ of 20 V and $I_{ds}$ of 10 A are 4.13 mΩ·cm$^2$ and 4.25 mΩ·cm$^2$ for the conventional and proposed MOSFETs, respectively. However, it was discovered that for $V_{gs}$ of <20 V, the drain current of the proposed MOSFETs starts to saturate at a lower drain voltage when compared to that of the conventional MOSFETs. It should be noted that the depletion region in the JFET region of a MOSFET has different behaviors as a function of gate voltage. The proposed MOSFETs have a deeper p-well junction, resulting in a larger depletion region during the forward conduction. At low gate voltages, a much larger depletion region occurs within the proposed MOSFETs. This larger depletion region constricts the current flow due to the reduction in the effective JFET width. The reduced effective JFET width of the proposed MOSFETs prevents the movement of electrons, resulting in the current reduction at lower gate voltages and thus higher $R_{on,sp}$. However, at $V_{gs}$ of 20 V, the effective JFET width is sufficient to accommodate high current in the proposed MOSFETs, and thus a lower $R_{on,sp}$ is achieved to match that of conventional MOSFETs. This mechanism of lower saturation current results in the improvement of SC ruggedness with no negative effect on $R_{on,sp}$. 

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Fig. 8.5. Short-circuit waveforms of the proposed MOSFETs. SC condition was $R_g$ of 20 $\Omega$, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V. The proposed MOSFETs achieved SCWT of 8 $\mu$s.

The measured forward blocking mode characteristics of the conventional and proposed MOSFETs are shown in Fig. 8.4. The high breakdown voltages with low leakage currents were achieved thanks to the efficient edge termination technique (Hybrid-JTE) and expertly optimized cell structures.

The short-circuit waveforms of the proposed MOSFETs are shown in Fig. 8.5. The measurement for short-circuit was conducted under the following conditions: $R_g$ of 20 $\Omega$, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V. Fig. 8.6 shows the drain current of the conventional and proposed MOSFETs under SC condition. The maximum drain current decreases by ~2.7 times, compared
to conventional MOSFETs, when using the proposed structure due to a deeper P-well, resulting in
the reduction in junction temperatures in the SiC MOSFET. Due to lower junction temperatures,
resulting in the small positive temperature feedback, the drain current of the proposed MOSFETs
exhibits a gentle slope after the maximum drain current is reached during the SC event. This low
junction temperature contributes to the improvement of SC ruggedness, which is \( \sim 4 \) times longer
than conventional MOSFET structure; Proposed MOSFETs achieved SCWT of 8 \( \mu \)s.

Fig. 8.7 shows the current density distribution of the simulated MOSFETs under (a) forward conduction (\( V_{gs} \) of 20 V and \( V_{ds} \) of 1 V) and (b) SC conditions (\( V_{gs} \) of 20 V and \( V_{ds} \) of 800 V).
The proposed MOSFETs have a deeper junction, resulting in a larger depletion region during the
forward conduction. Although the proposed MOSFETs have a narrower JFET width, the current
density is almost identical to that of the conventional MOSFETs during the conduction behaviors,
as shown in Fig. 8.7 (a). However, during short-circuit conditions, a much narrower and deeper
JFET region is achieved in the proposed MOSFETs, as shown in Fig. 8.7 (b). This significantly
increases JFET resistance, which suppresses the saturation current under SC conditions.
The trade-off relationship between $R_{on,sp}$ and SCWT was significantly improved by the proposed structure with a deep P-well. A novel approach to improve SCWT with no impact on $R_{on,sp}$ enables the decrease of the saturation current under high drain bias. Thus, the channeling implantation resolves the previous limitation of conventional MOSFETs and improves the trade-off between $R_{on,sp}$ and SCWT.

8.4. CONCLUSION

1.2 kV SiC MOSFETs achieving long SCWT with no negative effect on $R_{on,sp}$ was firstly proposed and demonstrated by applying channeling implantation to form a deep P-well. Under the operation condition for forward conduction, the conventional and proposed MOSFETs have almost identical $R_{on,sp}$. However, the maximum drain current of the proposed MOSFETs during the SC event was reduced by ~2.7 times, resulting in the increase of SCWT, which is ~4 times longer than the conventional MOSFETs. Chiefly, the trade-off relationship between $R_{on,sp}$ and SCWT was significantly improved.

8.5. ACKNOWLEDGMENT

The authors would like to thank SiCamore Semi, Bend, OR for the fabrication of the devices. The authors acknowledge that the channeling implantations for the proposed devices were conducted by NISSIN ION EQUIPMENT CO.,LTD., Kyoto, Japan. The authors would like to thank Mr. Takashi Kuroi and Mr. Nobuhiro Tokoro, and the team for the valuable discussion on the principle of channeling implantation.
8.6. REFERENCES


Chapter 9

Development of 1.2 kV 4H-SiC MOSFETs with Short Channel Length

9.1. INTRODUCTION

The research direction for 4H-SiC MOSFETs has mainly focused on reducing the specific on-resistance ($R_{on,sp}$) through improved channel mobility. The post oxidation annealing in nitric oxide (NO) ambient [1], accumulation mode channel [2], and high-quality epitaxial channel [3], [4] have been successfully implemented to improve channel mobility. However, the channel resistance still accounts for a large portion of the total on-resistance of 1.2 kV SiC MOSFETs despite many efforts to increase channel mobility [5]. To further improve the channel resistance, short channel lengths are preferable. However, short channel lengths result in high leakage current from the channel under blocking-mode operation, causing a reduction in breakdown voltage (BV) [5]. Additionally, shorter channel lengths result in poor short-circuit characteristics (e.g. short-circuit withstand time, SCWT) due to the larger saturation currents. In order to break the conventional trade-off relationship between $R_{on,sp}$ and BV or SCWT, SiC MOSFETs with short channel (0.3 μm) and deep P-well (1.8 μm) are proposed.

This paper presents 1.2 kV 4H-SiC MOSFETs with deep P-well utilizing channeling implantation to enable short channel length [6]. The channeling implantation was used to form deep junctions without using MeV high energy implantation [6–8]. A deep P-well structure suppresses the leakage current from the channel under the blocking-mode of operation, resulting in the improvement of the trade-off relationship between $R_{on,sp}$ and BV. Moreover, long SCWT was achieved from the MOSFETs with deep P-well despite the short channel lengths. Output,
Fig. 9.1. The cross-sectional view of (a) conventional and (b) proposed 1.2 kV MOSFETs.

Table 9.1. Design description of the fabricated 1.2 kV MOSFETs

<table>
<thead>
<tr>
<th></th>
<th>P-well depth</th>
<th>Channel length</th>
<th>$R_{on,sp}$ [mΩ·cm$^2$]</th>
<th>BV [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>~0.7 μm</td>
<td>0.3 μm</td>
<td>3.25</td>
<td>263</td>
</tr>
<tr>
<td>D2</td>
<td>~0.7 μm</td>
<td>0.4 μm</td>
<td>3.47</td>
<td>992</td>
</tr>
<tr>
<td>D3</td>
<td>~0.7 μm</td>
<td>0.5 μm</td>
<td>3.74</td>
<td>1669</td>
</tr>
<tr>
<td>D4</td>
<td>~1.8 μm</td>
<td>0.3 μm</td>
<td>3.35</td>
<td>1609</td>
</tr>
<tr>
<td>D5</td>
<td>~1.8 μm</td>
<td>0.4 μm</td>
<td>3.76</td>
<td>1608</td>
</tr>
<tr>
<td>D6</td>
<td>~1.8 μm</td>
<td>0.5 μm</td>
<td>4.12</td>
<td>1615</td>
</tr>
</tbody>
</table>

*R$_{on,sp}$ was extracted at $V_{gs}$ of 20V and $V_{ds}$ of 0.1V. BV was extracted at $I_{ds}$ of 1 mA.

blocking, and short-circuit characteristics measured from fabricated 1.2 kV 4H-SiC MOSFETs are presented. In addition, Sentaurus 2D TCAD was used to support and clarify the experimental results.

9.2. DEVICE STRUCTURE

Fig. 9.1 (a) and (b) show the cross-sectional view of the conventional and proposed MOSFETs, respectively. The channel length ($L_{ch}$) was varied to investigate the trade-off between $R_{on,sp}$ and BV or SCWT. $L_{ch}$ of 0.3, 0.4, and 0.5 μm were designed keeping other design rules the
Fig. 9.2. Net doping profile (A-A’ shown in Fig. 9.1) for the conventional MOSFETs using SPROCESS [9]. The conventional MOSFETs are composed of the conventional random implant. The accumulation mode channel and current spreading layer (CSL) were designed.

* The depth of channeling implants offers approximately 2.5 times deeper implant than that of the random implants using similar energy of Aluminum.

Fig. 9.3. Net doping profile (B-B’ shown in Fig. 9.1) for the proposed MOSFETs using SPROCESS [9]. The proposed P-well is composed of the conventional random implant as well as the channeling implant. The accumulation mode channel and CSL were designed.

same for both the conventional and proposed MOSFETs, as shown in Table 9.1.

The net doping profiles for the conventional and proposed MOSFETs are shown in Fig. 9.2 and Fig. 9.3, respectively. There are no additional photo mask processes to fabricate the proposed MOSFETs with deep P-well. For the fabrication of the deep JFET and P-well, the channeling
implant was added during the same implantation step as the conventional random implantation. The 4H-SiC (0001) substrates used in this study are with 4 degrees off toward $<11-20>$ direction. Therefore, to conduct the channeling implantation, a tilt angle of 4 degrees was applied to align Al implants with $<$0001$>$ direction of 4H-SiC [6–8]. Fig. 9.4 shows the SEM cross-sectional view of the proposed 1.2 kV MOSFETs.

9.3. FABRICATION TECHNOLOGY

The MOSFETs were fabricated at SiCamore Semi, OR, U.S.A [6]. A 10 μm thick drift layer with an N-type doping concentration of $8 \times 10^{15}$ cm$^{-3}$ on an N+ 4H-SiC substrate was used for the fabrication of the 1.2 kV MOSFETs. Two wafers were used to fabricate both the conventional and proposed MOSFETs for a fair comparison. For the conventional MOSFETs, random implants for Aluminum and Nitrogen were used to form the P-well/P+ source/JTE, and JFET/N+ source, respectively. In order to fabricate the proposed MOSFETs, additional channeling implants for Aluminum and Phosphorus during the P-well and JFET implants were performed to form the deep
P-well and JFET regions, respectively. At the conclusion of all the implantation steps, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed, followed by a post oxidation anneal (POA) in NO ambient. N-type polysilicon was deposited and patterned for the formation of the gate. After, borophosphosilicate glass (BPSG) was deposited as interlayer dielectric (ILD), then patterned and etched to make ohmic contact regions. Nickel (Ni) was deposited on the frontside, followed by an RTA for the silicidation process. Next, unsilicided Ni metals were removed. Ni was then deposited on the backside, followed by RTA process at 1000 °C for 2 mins. The source and gate metal, based on Al, were deposited, patterned, and etched. For the passivation, Silicon nitride was deposited, patterned, and etched. Finally, a solderable metal stack was deposited on the backside.

9.4. EXPERIMENTAL RESULTS AND DISCUSSIONS

The measured forward blocking characteristics of the conventional and proposed MOSFETs are shown in Fig. 9.5. For the proposed MOSFETs, the high breakdown voltages with the low
leakage currents were achieved regardless of channel lengths, whereas conventional MOSFETs with short channel (0.3 μm (D1) and 0.4 μm (D2)) show very large leakage current. The breakdown voltages of the proposed MOSFETs are governed by avalanche behaviors, not leakage current from the channel. In contrast to the proposed MOSFETs, significant leakage currents occur with the reduction in the channel length in the conventional MOSFETs. The blocking behaviors of the conventional MOSFETs with shorter channel lengths are determined by the leakage current from
the channel, rather than avalanche behavior. The deeper P-well increases the channel potential under the high drain voltages, contributing to suppressing the leakage current from the channel.

Fig. 9.6 (a) shows the measured output characteristics of the proposed MOSFETs with a channel length of 0.3 μm (D4). Output characteristics at V_{gs} of 20 V of the fabricated MOSFETs with different channel lengths are shown in Fig. 9.6 (b). The conventional MOSFETs offer better conduction behaviors for the same channel length because the proposed MOSFETs have a higher JFET resistance component due to the deeper P-well. However, the reduced channel lengths in the proposed MOSFETs substantially improve R_{on,sp} due to the low channel resistance, while maintaining high BV. Although the shorter channel lengths provide better conduction behaviors, D1 and D2 have low BV because of the high leakage currents. However, D4 allows high BV with low leakage currents. In consequence, R_{on,sp} was improved by approximately 10 % using D4 when compared to D3.

Fig. 9.7 shows the trade-off relationship between R_{on,sp} and breakdown voltage of the fabricated MOSFETs. As shown, the trade-off relationship was significantly improved using the deep P-well structure. Most importantly, the reduction in R_{on,sp} was achieved with no negative impact on the breakdown voltages when using shorter channel lengths with deeper P-well.

In order to further explore the effect of channel length in the conventional and proposed MOSFETs under the blocking behavior, simulated electrostatic potential near the surface, starting at the N+ source, proceeding through the channel, and ending in the JFET region (C-C’ shown in Fig. 9.1) was extracted at V_{ds} of 1200 V, as shown in Fig. 9.8. The wider and higher channel potential were achieved in the proposed structure when compared to the conventional MOSFETs. Although the channel potential of D3 and D4 is similar, D4 has a lower low leakage current at V_{ds}
Fig. 9.7. Trade-off relationship between $R_{on,sp}$ and breakdown voltage of the fabricated MOSFETs.

Fig. 9.8. Simulated electrostatic potential at channel region of the conventional and proposed MOSFETs with different channel lengths at $V_{ds}$ of 1200 V. This is because the potential in the JFET region of the proposed MOSFETs is lower than that of the conventional MOSFETs, as shown in Fig. 9.8. The lower JFET potential near the channel results in smaller leakage current in the proposed structures.

Fig. 9.9 (a) and (b) show the simulated electric field distribution at $V_{ds}$ of 1200 V of the conventional and proposed MOSFETs, respectively. The maximum electric field on the gate oxide
Fig. 9.9. Electric field distribution of the simulated (a) conventional and (b) proposed MOSFETs at $V_{ds}$ of 1200 V.

Fig. 9.10. Short-circuit waveforms of the proposed MOSFETs; channel length of (a) 0.3 $\mu$m (b) 0.4 $\mu$m, and (c) 0.5 $\mu$m. Short circuit test condition: $R_g$ of 20 $\Omega$, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V.

$(E_{ox})$ was extracted at the middle of the JFET region. By using a deep P-well structure, the maximum electric field directly beneath the gate oxide ($E_{ox}$) was 2.5 times reduced.

Short-circuit (SC) waveforms of the proposed MOSFETs; channel length of (a) 0.3 $\mu$m, (b) 0.4 $\mu$m, and (c) 0.5 $\mu$m are shown in Fig. 9.10. SC characteristics were measured at $R_g$ of 20 $\Omega$, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V. Regardless of the channel length, significantly improved short-circuit withstand time (SCWT) was achieved in the proposed MOSFETs due to the deeper P-well [6]. Shorter channel lengths have a larger maximum drain current during the SC condition due to the lower $R_{on,sp}$, as shown in Fig. 9.11. As a result, SCWT decreases with the reduction in $L_{ch}$ due
to this large drain current, resulting in high junction temperatures. Although the proposed MOSFETs with shorter channel lengths still show a trade-off relationship between $R_{on,sp}$ and SCWT, thanks to the deep P-well structure, the trade-off relationship was significantly improved in the proposed MOSFETs.

9.5. CONCLUSION

1.2 kV 4H-SiC MOSFETs achieving high breakdown voltage with low leakage currents were proposed and demonstrated by applying channeling implantation to form a deep P-well. Under the blocking-mode operation, the deep P-well structure effectively protects the channel region, resulting in the suppression of the leakage current. Consequently, $R_{on,sp}$ was reduced by approximately 10 % using the proposed MOSFETs with $L_{ch}$ of 0.3 μm when compared to the conventional MOSFETs with $L_{ch}$ of 0.5 μm. The maximum $E_{ox}$ under the blocking-mode operation was also 2.5 times reduced in the proposed MOSFETs. In addition, the trade-off relationship between $R_{on,sp}$ and SCWT was significantly improved by using the proposed MOSFETs.
9.6. ACKNOWLEDGMENT

The authors would like to thank SiCamore Semi, Bend, OR for the fabrication of the devices. The authors acknowledge that the channeling implantations for the proposed devices were conducted by NISSIN ION EQUIPMENT CO., LTD., Kyoto, Japan. The authors would like to thank Mr. Takashi Kuroi and Mr. Nobuhiro Tokoro, and the team for the valuable discussion on the principle of channeling implantation.

9.7. REFERENCES


Chapter 10

Development of Split-Gate 1.2kV 4H-SiC MOSFET with a Deep P-well

10.1. INTRODUCTION

Silicon Carbide (SiC) MOSFETs are highly desirable due to their faster switching characteristics and lower conduction loss when compared to Silicon (Si) IGBTs [1]. For high-frequency applications, MOSFETs with low reverse transfer capacitance ($C_{GD}$) and gate-to-drain charge ($Q_{GD}$) are required. In order to reduce $C_{GD}$ and $Q_{GD}$, the 4H-SiC Split-Gate (SG) MOSFETs [2] and Buffered-Gate (BG) MOSFETs [3] have been proposed and demonstrated. While the SG-MOSFETs offer improved $C_{GD}$ and $Q_{GD}$ without increasing the specific on-resistance ($R_{on,sp}$), the exposed edge of Poly-Si increases the electric field in gate oxide under the blocking characteristics, which may cause potential reliability issues related to gate oxide. In contrast, BG-MOSFETs achieve significantly reduced $C_{GD}$ and $Q_{GD}$ without reliability issues, but a much higher $R_{on,sp}$ has been observed.

This paper proposes a 1.2 kV 4H-SiC SG-MOSFET with a deep P-well structure to effectively reduce the electric field in the gate oxide, $C_{GD}$, and energy loss for switching characteristics. It is noted that MOSFETs with deep P-well structure exhibit improved ruggedness, as reported in [4]. To achieve a deep junction using low implantation energy, the proposed SG-MOSFETs were fabricated using channeling implantation [4–6]. The JFET region in the proposed SG-MOSFETs was well optimized to minimize JFET resistance that arises from the deep P-well. The evaluation of the proposed SG-MOSFET included comparisons with a conventional MOSFET and a conventional SG-MOSFET, assessing static characteristics, short-circuit characteristics, reverse
Fig. 10.1. (a) The cross-sectional view of 1.2 kV 4H-SiC. (b) The cross-sectional SEM images of fabricated 4H-SiC MOSFETs.

transfer capacitances, and switching characteristics. To extract the electric field in the gate oxide and compare experimental and simulated results, 2D TCAD simulations were employed.

10.2. DEVICE STRUCTURE

Fig. 10.1 (a) shows the cross-sectional view of the 1.2 kV 4H-SiC MOSFETs; conventional, conventional SG, and proposed SG, each having half JFET width of 0.8 μm, a channel length of 0.5 μm, and cell pitch of 5.8 μm. In the SG-MOSFETs, the gate extension beyond the P-well (align margin between the P-well and gate) of 0.3 μm was designed for secure conduction and blocking characteristics. An insufficient alignment margin can lead to a higher $R_{on,sp}$ due to the loss of a one-sided channel, while a large alignment margin may result in a high electric field in the gate oxide.
Fig. 10.2. The measured output characteristics of fabricated (a) conventional MOSFETs and (b) all MOSFETs. At $V_{gs}$ of 20 V and $V_{ds}$ of 0.1 V, $R_{on,sp}$ of the MOSFET, SG-MOSFET, and SG-deep MOSFET are 4.11 mΩ·cm², 4.13 mΩ·cm², and 4.19 mΩ·cm², respectively. The substrate thinning process was not conducted. (c) The measured transfer characteristics of fabricated MOSFETs.
In order to address the aforementioned drawback of conventional SG-MOSFET, which is high electric field in the edge of the gate, a deep P-well structure is proposed. Implementing a junction depth deeper than 1 μm using conventional implantation technology in 4H-SiC is challenging due to the requirement of over 1 MeV energy. The concept of channeling implantation [4–6] was utilized in the fabrication of proposed SG-MOSFETs to overcome limitations associated with implantation energy in 4H-SiC. Fig. 10.1 (b) shows the cross-sectional SEM images of fabricated 1.2 kV 4H-SiC MOSFETs.

10.3. RESULTS AND DISCUSSIONS

Fig. 10.2 (a) shows the typical output characteristics of the conventional MOSFET. Fig. 10.2 (b) compares the measured output characteristics at V_{GS} of 20 V of all MOSFETs. As evident, near-identical R_{on,sp} was achieved for all three devices; at V_{gs} of 20 V and V_{ds} of 0.1 V, R_{on,sp} of the MOSFET, SG-MOSFET, and SG-deep MOSFET are 4.11 mΩ-cm², 4.13 mΩ-cm², and 4.19 mΩ-cm², respectively. The value of R_{on,sp} incorporates substrate resistance of 350 μm. Fig. 10.2 (c) shows the typical transfer characteristics of fabricated MOSFETs. The near-identical transfer characteristics were achieved; the extracted threshold voltage (V_{th}) of the MOSFET, SG-MOSFET, and SG-deep MOSFET is 2.4 V, 2.3 V, and 2.3 V, respectively.

The measured blocking characteristics of the fabricated MOSFETs are shown in Fig. 10.3 (a). The SG-MOSFETs have a high leakage current and low breakdown voltage. This is due to the variation in the potential barrier in the SG-MOSFETs during the blocking behaviors, as shown in Fig. 10.3 (b) and Fig. 10.4. When the gate in the middle of JFET is removed, the potential barrier in the channel decreases, and the potential in the JFET region increases. Moreover, unintentional misalignment during the process should also be considered, which causes the channel potential
Fig. 10.3. (a) The measured blocking characteristics of fabricated MOSFETs. (b) The simulated maximum electric field in gate oxide and channel potential at $V_{\text{DS}}$ of 1200 V as a function of misalignment between P-well and gate.

barrier to be lower. However, the SG-deep MOSFETs with misalignment provide a low leakage current since the deep P-well effectively protects the surface regions of the MOSFET, as shown in Fig. 10.4 achieving a high channel potential barrier and low JFET potential.
Fig. 10.4. Simulated electrostatic potential at channel region of the MOSFETs at $V_{DS}$ of 1200 V.

Fig. 10.5. The electric field distribution of the simulated MOSFETs at $V_{DS}$ of 1200 V.

Fig. 10.5 compares the simulated electric field distribution of the MOSFETs at $V_{DS}$ of 1200 V. The maximum electric field ($E_{OX}$) in gate oxide occurs in the middle of the JFET region in MOSFET ($E_{OX}$ of 1.53 MV/cm). However, $E_{OX}$ of SG-MOSFET happens at the edge of the gate,
resulting in a much higher $E_{OX}$ (about 3× higher than MOSFET). However, the implementation of a deep P-well structure presents a significant advantage in terms of $E_{OX}$ reduction, exhibiting a 1.78× decrease compared to SG-MOSFET due to the improved shielding effect provided by the deep P-well structure, effectively suppressing the potential in the JFET region.

Fig. 10.6 shows the measured drain current of the MOSFETs under short-circuit (SC)
Table 10.1. Summary of experimental results.

<table>
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<th>MOS</th>
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<th>SG-Deep MOS</th>
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<td>$R_{on,sp}$ [mΩ-cm²]</td>
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<td>4.13</td>
<td>4.19</td>
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<tr>
<td>$V_{th}$ [V]</td>
<td>2.4</td>
<td>2.3</td>
<td>2.3</td>
</tr>
<tr>
<td>$BV$ [V]</td>
<td>1641</td>
<td>1495</td>
<td>1585</td>
</tr>
<tr>
<td>$E_{ox}$ [MV/cm]</td>
<td>1.53</td>
<td>4.64</td>
<td>2.61</td>
</tr>
<tr>
<td>(simulated)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCWT (μs)</td>
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<td>1.9</td>
<td>2.9</td>
</tr>
<tr>
<td>$C_{iss,sp}$ [nF/cm²] @ $V_{ds}$ of 400V</td>
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<td>25.8</td>
<td>29.8</td>
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<tr>
<td>$C_{oss,sp}$ [nF/cm²] @ $V_{ds}$ of 400V</td>
<td>1.43</td>
<td>1.44</td>
<td>1.43</td>
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<tr>
<td>$C_{rss,sp}$ [pF/cm²] @ $V_{ds}$ of 400V</td>
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<td>$R_{on} \times C_{rss}$ [mΩ-pF]</td>
<td>1434</td>
<td>847</td>
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<tr>
<td>$E_{on}$ [μJ]</td>
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<td>409</td>
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<tr>
<td>$E_{off}$ [μJ]</td>
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<td>230</td>
<td>153</td>
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<tr>
<td>$E_{total}$ [μJ]</td>
<td>721</td>
<td>639</td>
<td>611</td>
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conditions. The short-circuit characteristics were evaluated at $V_{gs}$ of 20 V and $V_{ds}$ of 800 V. To obtain the exact short-circuit withstand time, the gate pulse width increases by 0.1 μs until the device fails. SG-MOSFET shows an identical short-circuit withstand time (SCWT) when compared to MOSFET although it has a slightly higher maximum drain current. Due to the suppression of the current in the JFET region [4], the SCWT of SG-deep MOSFET increases by 1.52x when compared to MOSFET and SG-MOSFET.

The measured capacitance of the MOSFETs is shown in Fig. 10.7. The output capacitance of the devices was identical. SG-MOSFETs provide smaller reverse transfer capacitance due to the smaller gate-drain regions, as shown in Table 10.1. Moreover, due to the larger lateral straggling resulting from both random and channeling implantation conducted in the SG-deep MOSFET, the SG-deep MOSFET has a narrower JFET width than SG-MOSFET, providing lower $C_{rss}$ and slightly higher $C_{iss}$. Furthermore, the deep P-well structure offers low $C_{rss}$ under high drain voltages due to the deep junction after pinching off the JFET region.
Fig. 10.8. The measured switching waveforms of SG-deep MOSFET; (a) turn-on transient and (b) turn-off transient.

Fig. 10.8 shows the measured switching waveforms of the SG-deep MOSFET; (a) turn-on transient and (b) turn-off transient. A double pulse test was conducted to evaluate the switching characteristics of the devices using a DC supply voltage of 800 V. The off/on gate voltage of -4/20
V, respectively, was applied with $R_g$ of 20 Ω for the switching test. The calculated switching energy is summarized in Table 10.1. In the SG-deep MOSFET, $E_{on}$ increases by approximately 10% when compared to the SG-MOSFET. However, $E_{off}$ decreases by 1.5× due to low $C_{rss}$ compared to the SG-MOSFET. As a result, $E_{total}$ of 18% and 5% was reduced when compared to MOSFET and SG-MOSFET, respectively.

Table 10.1 summarizes the experimental results. An almost identical $R_{on,sp}$ and $V_{th}$ were achieved for the proposed MOSFETs. The SG-deep MOSFET improves the BV and $E_{OX}$ by 1.06× and 1.78× respectively when compared to the SG-MOSFET. Moreover, the SCWT of SG-deep MOSFET was significantly improved due to the deep P-well structure. High-frequency figures-of-merit (HF-FOM) are extracted using $[R_{on} \times C_{rss}]$ [2], [3]. The SG-deep MOSFET improves $[R_{on} \times C_{rss}]$ by 2.66× when compared to the conventional SG-MOSFET and thus reduces $E_{off}$ and $E_{total}$ by 1.5× and 1.05× respectively. Since some applications that use zero-voltage-switching are governed by turn-off energy loss, turn-off energy loss is much more crucial than turn-on energy loss [7]. It is demonstrated that the proposed SG-deep MOSFET improves the blocking behaviors, short-circuit characteristics, and switching characteristics by adopting the deeper P-well structure.

10.4. CONCLUSION

In this paper, we propose a 1.2 kV 4H-SiC SG MOSFET with a deep P-well structure. Channeling implantation with low energy was employed to form the deep junction. Through a comprehensive comparison with MOSFET and SG-MOSFET, the proposed SG-deep MOSFET demonstrates superior blocking characteristics (BV and $E_{ox}$), short-circuit characteristics, reverse transfer capacitance, and switching characteristics. As a result, the deep P-well junction in SG MOSFET is a suitable device for high-frequency and reliable applications.
10.5. ACKNOWLEDGMENT

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10.6. REFERENCES


Chapter 11

Demonstration of Novel 1.2 kV 4H-SiC JBSFETs (Junction Barrier Schottky diode integrated MOSFETs) with Deep P-well

11.1. INTRODUCTION

The operation of the inherent PN body diode in the 4H-SiC MOSFET structure is undesirable due to the BPD related degradation issues as well as the considerable reverse recovery current [1], [2]. An external SiC Junction Barrier Schottky diode (JBS diode) has been utilized in parallel with the SiC MOSFET as a freewheeling diode in power converter applications to disable the body diode within the MOSFET structure. External diodes take up additional space within a multi-chip package or power module, and result in parasitic inductance to the power loop during commutation events of the power converter.

A diode-integrated MOSFET (DioMOS) [3] and a monolithic integration of the Schottky diode with the SiC MOSFET (JBSFET) [4–7] have been proposed and demonstrated as an alternative. However, a very thin and heavily doped epitaxially grown channel is required to fabricate DioMOS, which makes the process complex and less controllable. Also, DioMOS possesses a critical drawback in that negative gate voltages cannot be used during the third quadrant operation. The JBSFETs from [4], [5] show higher specific on-resistance because of the larger cell pitch due to the inclusion of the Schottky area when compared to the pure MOSFET. AIST [8] and Toshiba [9] reported the importance of the optimization of JBSFETs. The reduced cell pitch of JBSFETs is required to achieve not only the reduced $R_{on,sp}$ but also deactivation of the body diode. In order to improve $R_{on,sp}$, intermittent placement of the JBS diode portions (Schottky regions) in the orthogonal direction of the JBSFET layout has been reported [6]. Despite many
efforts to improve the characteristics of the JBSFET, the forward conduction characteristics have still been unsatisfactory.

In this paper, an innovative layout approach for 1.2 kV JBSFETs is proposed and demonstrated to achieve identical cell pitch with the pure MOSFET. In order to further minimize cell density, the highly doped JFET implantation is implemented. In addition to the novel layout approach, the proposed JBSFET is featured by 1) enhanced doping in the JFET region, 2) thus very tight widths of JFET/Schottky regions, and 3) a 1.8 µm deep P-well and CSL (current spreading layer) implemented by the channeling implantation [10–13]. As a result, the proposed JBSFET offers the same static performances as the pure MOSFET, while boasting JBS diode-like 3rd quadrant current-voltage characteristics. The device design, layout approaches, fabrication, and static and short-circuit characteristics of the 1.2 kV 4H-SiC JBSFETs and MOSFETs are discussed.

11.2. DEVICE DESIGN AND FABRICATION TECHNOLOGY

When being integrated within the planar MOSFET cell structure, the Schottky region is generally allocated by interrupting the P-well and/or P+ source in the MOSFET cell. Therefore, the ‘stripe patterned’ layout of the Schottky region results in a large increase in the cell pitch of the JBSFET [4–6]. In the previous approach, due to the inclusion of the Schottky region and P+grid (P+source), the cell pitch of the stripe patterned JBSFET becomes 5 µm larger than that of the standalone MOSFET having the cell pitch of 5.6 µm, which brings about 89% increase in the cell pitch [4].

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Fig. 11.1. (a) The cross-sectional view and (b) layout approach of the proposed JBSFET with the innovative design. The cell pitch is 5.0 μm. (c) The cross-sectional view and (d) layout approach of the pure MOSFET. The cell pitch is 5.0 μm.

In order to reduce the cell pitch, placing the Schottky area in the orthogonal direction was proposed [6]. Using the same design rule as the stripe patterned JBSFET, the orthogonal JBSFET achieves a 2 μm reduction in the cell pitch, which makes its cell pitch still 53% larger than MOSFET. Although the 2 μm reduction in the cell pitch improves the forward conduction current, the $R_{on,sp}$ of the orthogonal JBSFET is still 22% higher than that of a standalone MOSFET [6].
For further reduction in the cell pitch of the JBSFET, an innovative layout approach is proposed, as shown in Fig. 11.1 (a) and (b). Fig. 11.1 (c) and (d) show the cross-sectional view and layout schematic of the pure MOSFET. In the proposed JBSFET design, the removal of the P+ source implant in the horizontal direction allows a significant reduction in the cell pitch (cut B-B’ in Fig. 11.1 (a) and (b)). The biasing for the P-well is provided by the P+ source in the longitudinal direction. Moreover, the widths of the JFET region and the Schottky area were decreased by enhancing the JFET doping concentration (N_{JFET}). Previous JBSFET [6] used the N_{JFET} of approximately 4\times10^{16} \text{cm}^{-3} and thus the half JFET width of 0.7 \mu\text{m} and half Schottky width of 1.0 \mu\text{m} were optimum. However, in this work, the half JFET width of 0.4 \mu\text{m} and half Schottky width of 0.6 \mu\text{m} are enabled with the increased N_{JFET} of approximately 8\times10^{16} \text{cm}^{-3}. As a result, the proposed JBSFET achieves the same cell pitch of 5.0 \mu\text{m} as the pure MOSFET does.

The tight cell pitch accomplished by the proposed approaches would directly improve the on-resistance. However, the enhanced JFET doping in the Schottky region may cause a large leakage current under the blocking mode due to the increase of the electric field at the Schottky contact [14] although the Schottky width was reduced. To suppress the leakage current due to the Schottky barrier lowering in the JBSFET, a deeper P-well structure was adopted [13]. The Aluminum channeling implantation at a tilt angle of 4 degrees with a low implantation energy (350 keV) was utilized to make a 1.8 \mu\text{m} deep junction of the P-well [10–13]. A phosphorus channeling implant was used to make a CSL under the P-well. The deeper P-well suppresses the electric field in the Schottky region, resulting in the leakage current under the blocking mode, which is discussed in the next section.

The MOSFETs and JBSFETs were included in the same mask set and were fabricated at SiCamore Semi, OR, U.S.A using the same process baseline described in [13]. After the formation
of ohmic contacts to both N+ and P+ sources, the ILD (interlayer dielectric) on the Schottky area was etched while etching the ILD on Polysilicon, making a contact to the top metal (Ti/TiN/AlCu; Ti forms Schottky on SiC). Thus, there is no additional process required to make the proposed JBSFET along with pure MOSFETs.

11.3. RESULTS AND DISCUSSIONS

Fig. 11.2 shows the measured output characteristics of the fabricated 4H-SiC JBSFET and MOSFET. As mentioned earlier, in the previous literatures, the stripe [4] and orthogonal [6] JBSFETs show 30% and 22% higher $R_{on,sp}$ than the pure MOSFETs due to the larger cell pitch of the JBSFET from the inclusion of Schottky contact regions. However, there is no $R_{on,sp}$ difference between the proposed JBSFET and pure MOSFET thanks to the proposed design concept discussed in the previous section. The same cell pitch and thus identical on-resistance between the JBSFET and MOSFET indicate that the 1.2kV SiC JBSFET can offer 2x reduction in overall chip size when compared to the external connection of separate MOSFET and JBS diode.
The typical third quadrant characteristics of the fabricated 4H-SiC JBSFET and MOSFET are compared in Fig. 11.3 (a). JBSFET provides a significantly low voltage drop due to a knee voltage of approximately 0.9 V accomplished by using a Ti Schottky contact. In contrast to the pure MOSFET, the JBSFET exhibits similar 3Q behaviors with different gate voltages, indicating that the governing current conduction mechanism is the Schottky current. It should be noted that the increase of the Schottky regions can allow more Schottky current under the third quadrant behaviors with minimal impact on the first quadrant characteristics [15].
Fig. 11.4. (a) The cross-sectional view of simulated 1.2 kV JBSFETs with conventional (shallow) P-well and deep P-well. (b) The electric field on the Schottky contact of the simulated 1.2 kV JBSFETs with conventional (shallow) P-well and deep P-well.

Fig. 11.3 (b) shows the typical forward blocking characteristics of the fabricated devices. All devices have identical breakdown voltages. However, the JBSFET with shallow P-well has a high leakage current originating from the Schottky barrier lowering. Although the Schottky width was reduced, the enhanced JFET doping concentration increases the electric field at the Schottky interface, increasing the leakage current. The proposed deep channeling implanted P-well minimizes the electric field at the Schottky contact and suppresses the leakage current. Fig. 11.4 (a) shows the cross-sectional views of simulated 1.2 kV JBSFETs with conventional (shallow) P-well and deep P-well. Fig. 11.4 (b) compares the electric fields at the Schottky contacts; it was discovered that the maximum electric field at the middle of the Schottky contact drastically
Fig. 11.5. Short-circuit waveforms of the fabricated JBSFET.

decreases when using the deep P-well structure. Due to the reduction in the electric field, a very low leakage current from the proposed JBSFET with the deep P-well was achieved as shown in Fig. 11.3 (b).

Fig. 11.5 shows short-circuit (SC) waveforms of the fabricated JBSFET at $R_g$ of 20 $\Omega$, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V. The proposed JBSFET with deep P-well provides short-circuit withstand time (SCWT) of ~4 $\mu$s, which is a reasonably high value in 4H-SiC planar MOSFETs. As discussed in [13], a MOSFET with a deep P-well structure achieved a much-improved SCWT when compared to a conventional MOSFET with a shallower P-well [13]. The difference in SCWT between MOSFET and JBSFET with deep P-well structure is attributed to the different failure mechanisms: In the JBSFET, the leakage current from the Schottky region increases due to Schottky barrier lowering effect at extremely high temperatures of SC condition [16], [17]. Nevertheless, the proposed JBSFET with a deep P-well structure offers better SC characteristics than the conventional MOSFET with a shallow P-well. Additionally, the advanced gate control circuits can detect SC states, and safely shut down the 4H-SiC MOSFETs within a very short time.
of 3.0 μs [17], [18]. Therefore, the proposed JBSFET can be utilized as a promising power semiconductor device.

11.4. CONCLUSION

1.2 kV SiC JBSFETs achieving a low voltage drop under 3Q mode with no negative impact on $R_{on,sp}$ was proposed and experimentally demonstrated by an innovative cell optimization and layout approach. Moreover, the deep P-well was adopted to restrict the leakage current from the Schottky contact. The proposed JBSFET decreases the overall chip size by 2x without any negative effects on the static characteristics, resulting in the area efficiency. Consequently, the proposed 4H-SiC JBSFET becomes a promising and suitable power semiconductor device for power electronics applications.

11.5. ACKNOWLEDGMENT

The authors would like to thank SiCamore Semi, Bend, OR for the fabrication of the devices. The authors acknowledge that the channeling implantations for the proposed devices were conducted by NISSIN ION EQUIPMENT CO., LTD., Kyoto, Japan. The authors would like to thank Mr. Takashi Kuroi and Mr. Nobuhiro Tokoro, and the team for the valuable discussion on the principle of channeling implantation.

11.6. REFERENCES


[18] AN2017-04, Infineon Application Note, Revision 1.1, June, 2018
Chapter 12

Analysis for Short-Circuit Failure Mechanisms of 1.2 kV 4H-SiC MOSFETs and JBSFETs

12.1. INTRODUCTION

Junction Barrier Schottky diode integrated MOSFETs (JBSFETs) have been demonstrated to overcome issues associated with the inherent PN body diode of 4H-SiC MOSFETs as well as MOSFET issues pertaining to poor reverse recovery characteristics [1–3]. In previous literatures, it was difficult to fairly compare current-voltage characteristics of planar 1.2 kV 4H-SiC MOSFETs and JBSFETs due to the larger cell pitch of JBSFETs, resulting in a higher specific on-resistance ($R_{on,sp}$). Thanks to an innovative layout approach, the identical cell pitch was achieved, and thus the identical $R_{on,sp}$ was obtained in the recent generation of the planar JBSFETs [3]. Moreover, novel channeling implants were implemented to improve the short-circuit characteristics [3], [4].

This paper presents a comparison of short-circuit failure mechanisms of 1.2 kV 4H-SiC MOSFETs and Ti JBSFETs, which have the same cell pitch, and thus the same $R_{on,sp}$. By adopting a deep P-well structure, superior short-circuit characteristics were achieved in both structures. However, at the same channel density, different behaviors for short-circuit characteristics were obtained due to the leakage current from the Schottky contact in the JBSFETs. In order to elucidate the short-circuit failure mechanisms, non-isothermal mixed-mode 2D TCAD device simulations were utilized. Moreover, based on the experimental results and analyses, solutions to further improve the short-circuit capabilities of JBSFETs are proposed.
12.2. Device Design

Fig. 12.1 shows the layout approach and cross-sectional views of the MOSFETs and Ti JBSFETs with deep P-well (~1.8 μm deep) implemented by channeling implantations [3]. The removal of the P+ source implant in the horizontal direction in JBSFETs allows the same cell pitch as the MOSFETs [3]. The tight cell pitch of 5.0 μm for both MOSFET and JBSFET was accomplished through enhanced doping concentrations in the JFET region.

Fig. 12.1. The layout approach of the (a) MOSFET and (b) JBSFET, and (c) The cross-sectional views of A-A’, B-B’ from MOSFET (see (a)), and A-A’, C-C’ from JBSFET (see (b)).
12.3. Fabrication Technology

The MOSFETs were fabricated by SiCamore Semi, OR, U.S.A, using the same base process line [3], [4]. A 10 μm thick drift layer with an N-type doping concentration of $8 \times 10^{15} \text{cm}^{-3}$ on an N+ 4H-SiC substrate was used for the fabrication of the 1.2 kV MOSFETs and JBSFETs. The MOSFETs and JBSFETs were fabricated on the same, 4-inch wafer using the same mask set. Random implantation for Aluminum and Nitrogen was used to form the P-well/P+ source/JTE, and JFET/N+ source, respectively. Additional channeling implantation for Aluminum and Phosphorus during the P-well and JFET implantation were implemented for the formation of the deep P-well and JFET regions, respectively. At the conclusion of all the implantation steps, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed, followed by a post oxidation anneal (POA) in NO ambient. N-type polysilicon was deposited and patterned for the formation of the gate. After interlayer dielectric (ILD) was deposited, the ILD was then patterned and etched to make ohmic contact regions. Nickel (Ni) was deposited on the frontside, followed by an RTA for the silicidation process. Next, unsilicided Ni metals were removed and annealed by RTA. Ni was then deposited on the backside, followed by the same RTA process. After the formation of ohmic contacts to both N+ and P+ sources, the ILD (interlayer dielectric) on the Schottky area was etched while etching the ILD on Polysilicon, making a contact to the top metal (Ti/TiN/AlCu; Ti forms Schottky on SiC). Thus, there is no additional process required to make the JBSFET along with pure MOSFETs. The Schottky, source, and gate metal (Ti/TiN/AlCu) were deposited, patterned, and etched. For the passivation, Silicon nitride was deposited, patterned, and etched. Finally, a solderable metal stack was deposited on the backside.
12.4. RESULTS AND DISCUSSIONS

Fig. 12.2 (a) shows the typical output characteristics of the fabricated 1.2 kV 4H-SiC MOSFETs and JBSFETs. Due to the same cell pitch, identical conduction behaviors were achieved; the specific on-resistance ($R_{on,sp}$) of the MOSFETs and JBSFETs are 4.23 and 4.24 m$\Omega$-cm$^2$, respectively (On-wafer measurement; substrate resistance is included). $R_{on,sp}$ was extracted at $V_{gs}$ of 20 V and $V_{ds}$ of 0.1 V.

The measured third quadrant characteristics of the fabricated MOSFETs and JBSFETs are shown in Fig. 12.2 (b). Low knee voltage was achieved in the JBSFETs thanks to the operation of Ti Schottky contact before the body diode turned on. As a result, low forward voltage drop under third quadrant condition was achieved in the JBSFETs.

Fig. 12.3 shows the measured drain current of the fabricated MOSFETs and JBSFETs under short-circuit conditions. The short-circuit characteristics were evaluated at $R_g$ of 20 $\Omega$, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V. In order to obtain short-circuit withstand time (SCWT), the gate pulse width was increased until the devices fail. The MOSFETs achieved superior short-circuit characteristics due to the formation of the deep P-well structure [4]. Although the JBSFETs still provide a short circuit withstand time of $\sim$4 $\mu$s, which is a reasonably high value when compared to other 4H-SiC planar MOSFETs, a shorter SCWT was obtained when compared to the MOSFETs fabricated on the same wafer. After the maximum drain current occurs, the drain current starts decreasing due to the reduction in electron mobility at high temperatures. However, the reduction in the drain current of the JBSFETs is smaller than that of the MOSFETs. This is due to additional leakage current from the Schottky contact. The short-circuit current in the MOSFET flows only through the n$+$ source. However, for the JBSFETs, the current flows not only through the n$+$ source, but also through the Schottky contact (leakage current) under the short-circuit condition.
Fig. 12.2. (a) The measured output characteristics and (b) measured third quadrant characteristics of the fabricated 1.2 kV 4H-SiC MOSFETs and JBSFETs.

Fig. 12.3. The measured drain current of the fabricated MOSFETs and JBSFETs when the device is failure under short-circuit conditions. The short-circuit characteristics were evaluated at $R_g$ of 20 $\Omega$, $V_{gs}$ of 20 V, and $V_{ds}$ of 800 V.

In order to further elucidate the short-circuit failure mechanisms, non-isothermal device simulations were conducted. Fig. 12.4 (a) shows the simulated SC characteristics of the MOSFETs and Ti JBSFETs. Thanks to well-optimized thermal-related simulation models [5], [6], the simulated results match well with the experimental results (i.e. Fig. 12.3). As shown in Fig. 12.4,
Fig. 12.4. (a) Simulated drain current and maximum junction temperature of MOSFETs and JBSFETs under a short-circuit condition. (b) Simulated Schottky current and maximum junction temperature of JBSFETs under short-circuit conditions. (c) Current density distribution of the JBSFET (left) and MOSFET (right) under short-circuit conditions. The short-circuit characteristics were evaluated at $V_{gs}$ of 20 V and $V_{ds}$ of 800 V.

different short-circuit failure mechanisms happen in the MOSFETs and JBSFETs. The junction temperature in the JBSFETs at the failure is lower than that observed in the MOSFETs. The Schottky leakage current is strongly governed by the Schottky barrier height, the electric field at the Schottky surface, and the junction temperature [7–9]. Due to the low Schottky barrier height obtained from Ti contact, high leakage current from Schottky contact occurs at a relatively low temperature.
Fig. 12.5. (a) Simulated drain current and maximum junction temperature of MOSFETs and JBSFETs with different Schottky widths and metals under short-circuit conditions. (b) Simulated Schottky current and maximum junction temperature of JBSFETs with different Schottky widths and metals under short-circuit conditions. The short-circuit characteristics were evaluated at $V_{gs}$ of 20 V and $V_{ds}$ of 800 V.

Fig. 12.4 (b) shows the simulated Schottky current and the maximum junction temperature of the JBSFETs under short-circuit conditions. The Schottky current of the JBSFETs increases due to the increase of the junction temperature during the short-circuit condition. Even after the gate bias is removed, the Schottky current of JBSFETs does not diminish, as shown in Fig. 12.4 (b) and (c). Fig. 12.4 (c) shows the current density distribution of the JBSFETs and MOSFETs under short-circuit conditions. In the JBSFETs, the high leakage current flows through the Schottky regions as mentioned above. High temperatures cause an increase in the thermionic field emission (TFE), resulting in the increase of the leakage current from the Schottky contact during the short-circuit condition. In contrast to the JBSFETs, it should be noted that the MOSFETs failed due to the high current through the channel region, as shown in Fig. 12.4 (c). Due to the low potential barrier provided by the Schottky contact, and due to the high thermionic field emission through the Schottky contact at high temperatures, the JBSFETs failed at a lower junction temperature than the MOSFETs.

In order to further improve the short-circuit characteristics of JBSFETs, the leakage current
from the Schottky contact should be suppressed. Higher work function metals such as Ni, Au, or Pt can be utilized as Schottky metals [10], [11]. Moreover, the narrower Schottky width can be designed to reduce the electric field on the Schottky surface.

Fig. 12.5 (a) shows the simulated drain current and maximum junction temperature of the MOSFETs and JBSFETs with different Schottky widths and metals under short-circuit conditions. The short-circuit withstand time increases in the JBSFETs with narrow Schottky width or high work function metal due to the reduction in the electric field on the Schottky surface or the increase of SBH. Especially, the Ni JBSFETs achieved similar SCWT to the MOSFETs by suppressing the leakage current from the Schottky region. The simulated Schottky current of the JBSFETs with different Schottky widths and metals under short-circuit conditions is shown in Fig. 12.5 (b). Thanks to the reduction in the TFE, the failure junction temperature increases in the Ti JBSFETs with the Schottky width of 0.4 μm and Ni JBSFETs, resulting in longer SCWTs.

It should be noted that there is a trade-off relationship between the forward voltage drop during the third quadrant operation and the SC leakage current when either using a different Schottky
metal or design in the Schottky region. Fig. 12.6 shows simulated third quadrant characteristics of the MOSFETs and JBSFETs with different Schottky widths and metals. Ni for the Schottky results in a high knee voltage, and thus a high forward voltage drop. Ti JBSFETs with narrow Schottky width show identical knee voltage when compared to Ti JBSFETs with a Schottky width of 0.6 μm, but the forward voltage drop increases due to the increase of JFET resistance.

Due to the trade-off relationship between the third quadrant and SC characteristics, optimization of the Schottky region is required; Schottky metals with too high work function and narrow Schottky width should be avoided to achieve the lowest forward voltage drop.

12.5. CONCLUSION

The short-circuit failure mechanisms of 1.2 kV 4H-SiC MOSFETs and Ti JBSFETs were compared. To fairly compare the short-circuit characteristics of the planar 1.2 kV 4H-SiC MOSFETs and JBSFETs, an innovative layout approach was applied in the JBSFETs to achieve the same cell pitch to the MOSFETs. Moreover, channeling implantation was implemented to form a deep P-well structure to improve the short-circuit characteristics. Thanks to the deep P-well structure, long SCWT was achieved in both MOSFETs and JBSFETs. However, with the same channel density, the JBSFETs provide shorter SCWT compared to equivalent MOSFETs. The difference in the short-circuit characteristics between the MOSFETs and JBSFETs is due to the different short-circuit failure mechanisms; the JBSFETs failed in the Schottky region under short-circuit characteristics while the failure of the MOSFETs happens in the channel region. In order to improve the short-circuit characteristics of the JBSFETs, a narrow Schottky width and high work function metal are proposed.
12.6. ACKNOWLEDGMENT

The authors would like to thank SiCamore Semi, Bend, OR for the fabrication of the devices. The authors acknowledge that the channeling implantations for the proposed devices were conducted by NISSIN ION EQUIPMENT CO., LTD., Kyoto, Japan. The authors would like to thank Mr. Takashi Kuroi and Mr. Nobuhiro Tokoro, and the team for the valuable discussion on the principle of channeling implantation.

12.7. REFERENCES


Chapter 13

Development of 1.2 kV 4H-SiC Planar JBS Diode with Superior Reverse Characteristics

13.1. INTRODUCTION

The main advantages of Silicon Carbide (SiC) Junction Barrier Schottky (JBS) diodes are low forward voltage drop and fast recovery during the switching events [1]. Even though the P+ grids suppress the leakage current from the Schottky contact, the leakage current is still the main concern in regard to the design of the 4H-SiC JBS diode. To reduce the leakage current, high work function metals have been utilized to increase the Schottky barrier height (SBH) [2], [3]. Due to the trade-off relationship between the forward voltage drop and leakage current, the high SBH increases the forward voltage drop. Due to the limitation of P+ implantation depth, a shallow P+ grid has been formed in the planar JBS diode. This shallow P+ grid does not effectively shield the Schottky region, causing high leakage current. A breakthrough in the traditional trade-off relationship has been demonstrated with a trench JBS diode [4], [5]. The trench structure increases the depth of the P+ grid, helping suppress the leakage current [4], [5]. However, the breakdown voltage (BV) decreases since the effective epi-layer thickness decreases due to the trench structure [5]. Moreover, the trench grid structure not only requires complicated processes afterwards, but it also demands optimization of the edge termination, possibly requiring deep junction [5]. To overcome the limitation of the implantation depth, the concept of channeling implantation has been reported and demonstrated [6–9]. The channeling implantation for Aluminum provides approximately 2.5 times deeper junction than the conventional non-channeling direction implantation (random implantation) [6], [9]. By utilizing channeling implantation, low cost and high productivity can be
achieved through reduced implant energy and fewer implantation steps. Additionally, it allows for the formation of thin soft/hard masks, resulting in insensitivity to critical dimension (CD) and minimal loss of mask shape [6].

In this paper, a 1.2 kV 4H-SiC planar JBS diode with a deep P+ grid structure, implemented by channeling implantation, was designed and fabricated. Without the trench structure, a planar JBS diode with a junction depth of 2.2 μm was successfully fabricated using an implantation energy of 350 keV. The formation of the deep junction significantly suppressed the leakage current from the Schottky contact. Moreover, the relatively low doping concentrations of the deep region are largely depleted under the reverse blocking mode of operation, achieving a similar BV to the JBS diode with a shallow junction. The edge termination technology (Hybrid-JTE) for the deep and shallow junction depth was also discussed. Sentaurus 2D TCAD simulations were utilized to support the experimental results.

13.2. RESULTS AND DISCUSSIONS

Fig. 13.1 shows cross-sectional views of the 1.2 kV 4H-SiC JBS diodes; (a) JBS_0.8 μm, (b) JBS_1.4 μm, and (c) JBS_2.2 μm, each having a Schottky width of 2.0 μm and a P+ grid width of 2.0 μm. Titanium (Ti) is used as the Schottky metal. Fig. 13.1 (d) and (e) show the cross-sectional SEM images of the fabricated 1.2 kV 4H-SiC JBS diodes. Fig. 13.2 shows a designed P+ grid implant profile using process simulation (A-A’ shown in Fig. 13.1 (a)) [10]. A Monte Carlo simulation calibrated by Synopsys and NISSIN ION EQUIPMENT was utilized for the implant profile [6]. For JBS_0.8 μm, JBS_1.4 μm, and JBS_2.2 μm, the maximum implantation energies (implant type) are 350 keV(random), 580 keV (random), and 350 keV (channeling), respectively. With identical implantation energy, the channeling implantation provides 2.75 times deeper
Fig. 13.1. The cross-sectional view of 1.2 kV 4H-SiC JBS diode with the junction depth of (a) 0.8 μm, (b) 1.4 μm, and (c) 2.2 μm. The cross-sectional SEM images of the fabricated 1.2 kV 4H-SiC JBS diodes with the junction depth of (d) 0.8 μm and (e) 2.2 μm.

Fig. 13.2. Designed implant profiles for P+ grid using SPROCESS [10] (A-A’ shown in Fig. 13.1. (a)).

Due to the use of the deep junction with the channeling implantation, the previous limitation was resolved, eliminating the requirement of
Fig. 13.3. The measured forward I-V characteristics of fabricated 4H-SiC JBS diodes; chip size is 0.045 cm².

![Forward I-V Characteristics](image1)

Fig. 13.4. The measured reverse I-V characteristics of fabricated 4H-SiC JBS diodes.

![Reverse I-V Characteristics](image2)

trench structure.

Fig. 13.3 shows the measured forward I-V characteristics of the fabricated 4H-SiC JBS diodes. Identical knee voltage was achieved due to the identical Schottky metal. Although the deep P+ grid structure added additional resistance, almost identical forward voltage drop was obtained regardless of the depth of the P+ grid; the forward voltage drops at $I_F$ of 10 A of 1.72 V, 1.73 V, and 1.77 V, respectively were achieved in JBS_0.8 μm, JBS_1.4 μm, and JBS_2.2 μm. Since channeling implantation exhibits minimal lateral straggling, the resulting additional resistance from the deep P is negligible.

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Fig. 13.5. (a) The simulated cross-sectional view of current density, (b) electrostatic potential, electric field (c) through B-B’ shown in Fig. 13.1, and (d) through C-C’ shown in Fig. 13.1 of 4H-SiC JBS diodes under the reverse voltage of 1600 V.

The measured reverse I-V characteristics of the fabricated 4H-SiC JBS diodes are shown in Fig. 13.4. As the P+ grid gets deeper, the reverse leakage current becomes reduced. Especially, JBS_2.2 μm significantly suppresses the leakage current. The leakage currents at 1200 V are 60 μA, 1.5 μA, and 1.7 nA, respectively. It is important to note that the reduction in the breakdown voltage observed from JBS_2.2 μm is minimal thanks to the relatively low doping concentration in the deep junction, unlike the trench JBS diode. The proposed JBS diodes slightly decrease the
breakdown voltage since the space between the P+ region gets wider in the deep P region due to reduced lateral straggling from the channeling implantation compared to the random implantation.

In order to clarify the experimental results, a 2D simulation was conducted. Fig. 13.5 (a) shows the simulated cross-sectional view of the current density of the 4H-SiC JBS diodes. The leakage current from the Schottky is perfectly suppressed in JBS_2.2 μm. This is due to the relatively lower potential, reducing the electric field when compared to the shallow P+ grid, as shown in Fig. 13.5 (b). It is also demonstrated that the deeper P structure drastically reduces the electric field on the Schottky contact, as shown in Fig. 13.5 (c) and (d).
For high and stable breakdown voltage, Hybrid-JTE was utilized in all JBS diodes as the edge termination [11]. Fig. 13.6 shows the simulated breakdown voltages of the Hybrid-JTE with different main junction depths; an identical implant profile of JTE was utilized for the different devices. High breakdown voltages were achieved except for the junction depth of 2.2 μm with high doping concentration (~2×10^{18} cm^{-3}). Low breakdown voltage is attained due to the heavily doped, deep junction since the highest electric field occurs in the main junction at V_{ds} of 1200 V, as shown in Fig. 13.7. Edge termination relieves the electric field in the main junction, but it is not perfectly terminated. As a result, the depth of the JTE should be as deep as the main junction to achieve high breakdown voltage in the deep junction with high doping concentration. However, the deep junction depth with low doping concentration provides high breakdown voltage with the shallow junction depth of the JTE, which is the identical JTE profile and design to the conventional JBS diode. Since the low doping regions are largely depleted under the reverse characteristics, the undepleted deep P regions are closed to the shallow junction of P+. The utilization of a deep junction formed by channeling implantation resulted in two key advantages. First, a high breakdown voltage with a low leakage current, comparable to shallow junctions, was achieved due to minimal loss of the drift region from the largely depleted P region. Second, was the ability to utilize an identical edge termination process, simplifying the overall fabrication process.

Thanks to well-designed and optimized edge termination, the active areas from the JBS diodes with different junction depths are fairly compared in terms of the reverse characteristics. Identical knee voltage and forward voltage drop were achieved regardless of the P+ grid junction depth, whereas a significantly reduced leakage current was achieved in JBS_2.2 μm. In the trench JBS diode, the breakdown voltage decreases as much as the trench depth. However, the deep junction
using the channeling implantation which has low doping concentrations in the deeper side of the junction, is largely depleted under the reverse characteristics, minimizing the loss of the effective epi-layer, maintaining the high breakdown voltage. Moreover, due to large depletion in the deep P, under the reverse I-V characteristics, identical edge termination with shallow P depth can be utilized in the JBS diodes with deep P structure. By adopting the channeling implantation technique, the previous concerns for the JBS diode are perfectly resolved. As a result, the proposed JBS diodes can be utilized as a promising power device for power electronics applications.

13.3. CONCLUSION

A 1.2 kV 4H-SiC JBS diode with deep P+ grid structure is demonstrated in this paper. Channeling implantation with low energy was implemented in the proposed JBS diodes to achieve the deep junction. JBS diodes with various junction depths are compared with respect to the forward and reverse I-V characteristics. Similar forward characteristics were achieved regardless of the junction depth, but the leakage current was dramatically suppressed in the proposed JBS diodes with deep P structure. In order to support the experimental results, the simulated electric field on the Schottky region was extracted. The edge termination technology with different junction depths for 1.2 kV 4H-SiC devices is discussed. It is important to note that the proposed JBS diodes applying channeling implantation resolve the previous issues from the trench structure, which are low breakdown voltage, complicated process, and edge termination techniques.

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13.5. REFERENCES


Chapter 14

Summary and Future work

14.1. Summary

1.2 kV rated 4H-SiC power devices such as MOSFETs, JBSFETs, and JBS diodes have been extensively examined with optimizing and improving their static, dynamic, reliability, and ruggedness. The research work in this field has made significant contributions, which can be summarized as follows:

(1) Process optimization of 1.2 kV 4H-SiC MOSFET

1.2 kV 4H-SiC MOSFETs with different junction depths in the JFET and P-well regions have been the subject of investigation. The deep JFET structure offers a low specific on-resistance by reducing the spreading resistance, allowing for a narrow JFET width. Moreover, the feasibility of a narrow JFET width improves the trade-off relationship between specific on-resistance and short-circuit withstand time in the deep JFET region. On the other hand, the deep P-well structure enhances the blocking characteristics and enables a short channel length of 0.4 µm. To further enhance device performance and ruggedness, a combination of deep JFET and deep P-well structures has been proposed.

(2) Cell optimization of 1.2 kV 4H-SiC MOSFET

A comprehensive structural analysis of 1.2 kV 4H-SiC MOSFETs with an accumulation mode channel was conducted. Various cell designs were fabricated and evaluated, with a specific focus on their output, transfer, and blocking characteristics. All design parameters, including channel
length, JFET width, contact openings, gate-to-source overlap, and cell pitch were thoroughly investigated. It was observed that the channel resistance remains the primary factor influencing the performance of 1.2 kV 4H-SiC MOSFETs despite many efforts to enhance the channel mobility.

(3) Analysis for Cell Topologies of 1.2 kV 4H-SiC Planar MOSFET

Thorough investigations were carried out on the layout approaches and their impact on the static, dynamic, and short-circuit ruggedness characteristics of 1.2 kV 4H-SiC MOSFETs. Different layout topologies (linear and hexagonal) and different design variations (with and without bridge of P-well) were evaluated to assess their effect. The experimental results demonstrated that: 1) the hexagonal layout topology enables a low specific on-resistance, 2) the linear MOSFET exhibits excellent suitability for high-frequency applications due to its fast switching speed, and 3) the hexagonal topology with a bridge offers enhanced reliability and ruggedness.

(4) Optimization of 1.2 kV 4H-SiC MOSFET with channel diode

A comprehensive investigation was conducted on various channel design parameters to achieve unipolar operation under 3rd quadrant characteristics. These parameters included channel doping concentration, channel length, and different gate oxides. It was observed that all channel design parameters exhibit a trade-off relationship between 3rd quadrant operation mode and blocking characteristics. However, it was found that a channel length of 0.4 µm or a thin gate oxide provided optimum characteristics for the channel diode.
(5) A novel 1.2 kV 4H-SiC MOSFETs to improve short-circuit characteristics and blocking characteristics

The implementation of a deep P-well structure, achieved through channeling implantation, significantly enhances the trade-off relationship between specific on-resistance and short-circuit withstand time in 1.2 kV 4H-SiC MOSFETs. To address the limitations of previous implant energy, channeling implantation was employed. This novel structure provides approximately four times longer short-circuit withstand time compared to conventional MOSFETs without any negative impact on specific on-resistance. Additionally, it allows for a short channel length of 0.3 μm. The deep P-well structure effectively suppresses the leakage current from the channel region under forward blocking mode, resulting in high breakdown voltage with low leakage current. Consequently, the specific on-resistance is reduced by approximately 10% compared to a channel length of 0.5 μm.

(6) Improved static, dynamic, and ruggedness characteristics of 1.2 kV 4H-SiC Split-Gate MOSFET

The proposed 1.2 kV 4H-SiC Split-Gate (SG) MOSFETs with a deep P-well structure demonstrate improvements in blocking, switching, and short-circuit characteristics. A noteworthy reduction in the maximum electric field in the gate oxide is observed when compared to conventional SG MOSFETs. The low gate-drain capacitance results in a decrease in total switching loss. Furthermore, the deep junction contributes to an increase in short-circuit withstand time.

(7) A novel 1.2 kV 4H-SiC Schottky-integrated MOSFETs (JBSFETs)
The proposed 1.2 kV 4H-SiC Schottky-integrated MOSFETs (JBSFETs) demonstrate an identical specific on-resistance compared to pure MOSFETs. An innovative layout approach and a novel deep P-well structure are employed in the JBSFET design, allowing for an identical cell pitch to the pure MOSFETs. The leakage current originating from the Schottky contact is effectively suppressed by adoption of a 1.8 µm deep P-well structure implemented using channeling implantation. While JBSFETs offer a shorter short-circuit withstand time than MOSFETs due to the high leakage current from Schottky contact, it still reaches a reasonably high value of ~4 µs in 1.2 kV 4H-SiC MOSFETs. To improve the short-circuit characteristics of JBSFETs, solutions such as a narrow Schottky width and high work function metal are proposed.

(8) A novel 1.2 kV 4H-SiC Junction Barrier Schottky (JBS) diodes

To enhance the reverse characteristics, a novel 1.2 kV 4H-SiC JBS diodes employing a deep P+ grid structure were proposed and demonstrated. To achieve a deep junction with low implantation energy, channeling implantation was implemented. Diodes with different junction depths of the P+ grid (0.8 µm, 1.4 µm, and 2.2 µm) were fabricated to compare the forward and reverse I-V characteristics. Almost identical forward I-V characteristics were achieved regardless of the P+ grid depth. However, the leakage current was significantly suppressed with the deeper P+ grid junction depth; 60 µA, 1.5 µA, and 1.7 nA (at 1200V for 0.8, 1.4, 2.2 µm deep P+ grids, respectively). Despite the deep junction implemented through channeling implantation, the proposed JBS diode achieves high breakdown voltages similar to those of shallow junctions, thanks to the relatively low doping concentration in the deep junction. Furthermore, different edge termination structures with various main junction depths were discussed.
14.2. Future Work

Despite achieving low specific on-resistance, the 1.2 kV 4H-SiC planar MOSFETs fabricated in this study exhibit higher specific on-resistance compared to commercially available 1.2 kV 4H-SiC trench MOSFETs. Hence, the primary objective of future work is to further reduce the specific on-resistance of the planar MOSFETs.

First, the substrate resistance can be reduced by griding the substrate. In this study, a substrate thickness of 350 μm with a resistivity of 0.02 Ω·cm was utilized, resulting in a specific substrate resistance of 0.7 mΩ·cm². By thinning the substrate to 150 μm, the specific substrate resistance can be reduced to 0.3 mΩ·cm². Moreover, as discussed in Chapter 4, the channel resistance continues to be the predominant factor affecting the performance of 1.2 kV 4H-SiC planar MOSFETs. This is attributed to the low channel mobility of the planar MOSFETs. To enhance the channel mobility, in-depth investigations into gate oxide properties and the development of novel gate oxide technologies are essential.

The second area of future work involves verifying the uniformity of channeling implantation. Additionally, it is necessary to investigate the impact of the thickness of the screening oxide on channeling implantation.

In addition, the dV/dt capability of various edge termination structures and reliability tests, such as high temperature reverse bias (HTRB) and high temperature gate bias (HTGB), are of interest.

Lastly, 1.2 kV 4H-SiC trench MOSFETs will be designed and fabricated. Trench MOSFETs offer higher channel mobility and density, leading to improved conduction characteristics compared to planar MOSFETs. However, they face a critical issue of high electric field in the gate
oxide at the trench edge, which can reduce the breakdown voltage. Therefore, future work aims to develop trench MOSFETs with low specific on-resistance and a low electric field in the gate oxide.