State University of New York Polytechnic Institute
Colleges of Nanoscale Science and Engineering

Development of 4H-SiC SMART
(Scalable, Manufacturable, And Robust Technology)
Power ICs

A Dissertation Submitted in Partial Satisfaction of the Requirements
for the Degree of Doctor of Philosophy

in

Nanoscale Engineering

by

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2023
ABSTRACT

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The research primarily focuses on the design and development of SMART Power Integrated Circuits (ICs) in silicon carbide (4H-SiC). Over the past decades, power conversion has become more prevalent within the US as technological innovation has enabled the electrification of industrial systems, from energy to aerospace. Silicon (Si)-based power and CMOS devices have been the amicable semiconductor technology for power conversion. However, with the ever-evolving application space, the inherent material properties of Si hamper the capabilities in terms of power processing and high-temperature (HT) operation. The current generation power IC (multiple power integrated functions onto a single chip) technologies, predominantly Bulk-Silicon and Silicon-On-Insulator (SOI) technologies have limitations in their operational temperatures and power handling capability. Based on the theoretical limits, Si-based ICs are rated at 150 °C and are not operational beyond 200 °C due to leakage and reliability issues. Although SOI technology offers relief up to 300 °C, with the insulated region, it also fails beyond 300 °C. In recent decades, 4H-SiC has emerged as a reliable material for the development of high-voltage (HV) and high-temperature power devices. Due
to its superior material properties, 4H-SiC power devices can operate at high power and high temperatures when compared to their Si counterparts. In the current day scenario, Si-based power and control ICs drive the HV discrete 4H-SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), and this technology appendes to an increase in system footprint, and also in the parasitic effects from the interconnects hampering the reliability. Also, the high-temperature operation, one of the significant assets of 4H-SiC cannot be exploited. Hence, a single-chip 4H-SiC-based IC solution by monolithically integrating the HV Power MOSFET with low-voltage (LV) complementary metal-oxide-semiconductor (CMOS) can be a considerable solution to address the high power and extreme temperature challenges of the Si power ICs. The development of 4H-SiC-based power ICs is now seamlessly possible, thanks to considerable progress made over the last decade in material development and device fabrication. The exceptional advancements and the significant progress that was made in developing the technology platform for the demonstration of 4H-SiC Power ICs are reported in this dissertation.

The fundamental step in designing the technology roadmap of a semiconductor material is understanding the trade-off performances of that particular semiconductor. Hence a detailed trade-off analysis was reported that was conducted on 4H-SiC and other wide bandgap semiconductors (GaN, Ga2O3, and diamond). This analysis concluded by letting the designers know the criticality of meticulous scrutiny and cautious selection of impact ionization coefficients from the existing literature to ensure accurate assessment and optimization of trade-off performance parameters. Additionally, simplified generalized equations for both non-
punch-through (NPT) and punch-through (PT) design configurations to effectively design the drift layers in unipolar 4H-SiC power devices are documented.

2D-device, process simulations, and experimental demonstration of the HV lateral MOSFETs and diodes in 4H-SiC, specifically tailored for integration within power ICs are discussed. The cell designs, field management techniques, peripheral designs, and BV tailoring techniques of the HV lateral devices are reported in detail. The HV lateral devices are designed to operate at (400V-600V) and to be integrated with the Power ICs. The experimental results of the HV lateral devices demonstrate that the devices not only have the best-in-class $R_{on,sp}$ - BV trade-off performance but are also capable of handling large currents validating efficient cell and peripheral design techniques.

The design and analysis of critical module processes for CMOS development are also detailed. Channel engineering techniques (accumulation mode vs Inversion mode) are applied to match the threshold voltages ($V_{th}$) of the LV NMOS and PMOS. Multiple gate oxide recipes are developed to maximize the channel mobilities of electrons and holes. The results of the efforts dedicated to optimizing CMOS performance through improved ohmic contacts, including the investigation of metal contacts for simultaneous formation of n-type and p-type ohmic contacts were reported.

The critical need for high-voltage isolation in power IC technology to ensure safety, reliability, and proper functioning was addressed. The utilization of junction isolation through the P+ Isolation junction implemented via Aluminum channeling implantation has been experimentally verified to yield promising blocking voltages required for the reliable operation
of the ICs. Another HV isolation requirement which is the interlayer dielectric (ILD) voltage blocking between the adjacent metal layers carrying different voltage potentials is also addressed.

Building upon the developed CMOS technology, the performance of digital CMOS ICs at extreme temperatures up to 400 °C has been demonstrated, covering packaging flow, assembly process, employed materials, and encountered challenges during HT measurements. This successful performance of the CMOS ICs at extreme temperatures (400 °C) further confirmed the potential of 4H-SiC as a promising material for the development of high-temperature electronics.
DEDICATION

“Almighty God, who hast created man in Thine own image, and made him a living soul that he might seek after Thee and have dominion over Thy creatures, teach us to study the works of Thy hands that we may subdue the earth to our use, and strengthen our reason for Thy service.”

— James Clerk Maxwell, as cited in E.L. Williams and G. Mulfinger, 1974, p. 487

“This most beautiful system of the sun, planets, and comets, could only proceed from the counsel and dominion of an intelligent and powerful Being... This Being governs all things, not as the soul of the world, but as Lord over all; and on account of his dominion, he is wont, to be called Lord God παντοκράτωρ or Universal Ruler...”

— Sir Isaac Newton, The Principia: Mathematical Principles of Natural Philosophy

To my Lord and Savior Jesus Christ, my loving parents, and my wonderful sister
ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my Ph.D. advisor, Dr. Woongje Sung, for his invaluable guidance, support, and mentorship throughout this doctoral journey. His expertise, unwavering commitment, and dedication to academic excellence have been instrumental in shaping my professional growth. His insightful feedback, constructive criticism, and encouragement have continually pushed me to strive for excellence and explore new horizons in my field of study. I am truly grateful for his patience, understanding, and belief in my abilities, which have kept me going. Once again, I greatly appreciate my advisor for the opportunity given and for the faith in me. Thank you!

I would like to thank Dr. Spyridon Galis, Dr. Unnikrishnan Sadasivan Pillai, Dr. Bongmook Lee, and Dr. Anant K Agarwal for agreeing to be on my Ph.D. committee. Their mentorship has not only enriched the research work but also provided me with a deeper understanding of the field. I am truly grateful for their time, dedication, and valuable contributions to this research.

I would like to thank my lab members Nick Yun, Justin Lynch, Dongyoung Kim, Steve Manchini, Skylar DeBoer, and Dinuth Chamila Yapa Bandara Yapa Mudiyanselage for their support and valuable technical discussions. I would also like to thank my post-docs, Dr. Seung Yup Jang and Dr. Adam J Morgan, for their valuable insights and technical discussions.

It has been a pleasure working with Dr. Hua Zhang (now with Texas Instruments), Dr. Liu Tianshi (now with Ford Motor Company), Dr. Utsav Gupta (now with Texas Instruments), Emran Ashik (NC State university), Dr. Ayman Fayed and Dr. Anant K Agarwal from the Ohio State
University, and Dr. Bongmook Lee from SUNY Poly, Utica, Alexander Bialy from SUNY Poly, for the collaborative research work.

Finally, I would like to thank my parents and my sister for their love, encouragement, and relentless support throughout my life.
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CHAPTER 1: Introduction

1.1 The Benefit of Utilizing 4H-SiC

The electric power sector occupies a critical position within the broader energy consumption landscape, contributing to approximately 30% of primary energy consumption in the United States [1], as reported by the U.S. Energy Information Administration in the Monthly Energy Review (June 2023). In light of the nation's commitment to advancing energy sustainability, it becomes paramount to prioritize the enhancement of power electronic systems efficiency. Power electronic systems, encompassing converters, inverters, and motor drives, are pivotal in facilitating the efficient conversion, control, and distribution of electrical power. Consequently, advancements in power electronic systems hold immense potential for substantial improvements in energy efficiency. One indispensable element of any power electronic system is the semiconductor switching device, such as MOSFETs and IGBTs, which dictate the power levels and switching frequencies achievable within the electronic system. A significant proportion of losses in power electronic converters arises from dissipation in the power semiconductor devices themselves.

Table 1.1: Material properties of wide bandgap semiconductors in comparison with silicon

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Bandgap, $E_g$ (eV)</td>
<td>1.1</td>
<td>3.26</td>
<td>3.39</td>
<td>4.9</td>
<td>5.45</td>
</tr>
<tr>
<td>Dielectric constant, $\varepsilon$</td>
<td>11.8</td>
<td>9.7</td>
<td>9.0</td>
<td>10</td>
<td>5.7</td>
</tr>
<tr>
<td>Mobility, $\mu$ (cm²/V·s)</td>
<td>1400</td>
<td>950</td>
<td>1500</td>
<td>300</td>
<td>2000</td>
</tr>
<tr>
<td>Critical Electric field EC (MV/cm)</td>
<td>0.3</td>
<td>2.5</td>
<td>3.3</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Thermal Conductivity $\lambda$ (W/m·K)</td>
<td>1.5</td>
<td>3.7</td>
<td>2.1</td>
<td>0.13-0.23</td>
<td>10</td>
</tr>
</tbody>
</table>
Silicon (Si) has long been the preferred semiconductor material for power devices owing to its cost-effectiveness, ease of processing, and extensive knowledge of its material properties. Nonetheless, Si devices are gradually approaching their inherent limitations in terms of blocking voltage capability, operating temperature, and switching frequency [6]. This is primarily attributed to the intrinsic material properties of Si as shown in Table 1.1. To overcome these limitations, wide-bandgap (WBG) power semiconductors have emerged as a compelling alternative to Si due to their inherent material properties as outlined in Table 1.1. WBG materials predominantly 4H-SiC and GaN exhibit superior electrical properties, presenting an opportunity to develop power electronic systems with enhanced efficiency and higher power densities [2], [4]-[8].

![Figure 1.1: Wide band gap semiconductor applications and potential market](image)

Fig. 1.1 covers the applications and the potential market scope of GaN and 4H-SiC. Both GaN and 4H-SiC exhibit distinct characteristics, particularly in terms of electron mobility. GaN boasts an electron mobility of 2,000 cm²/V-s, making it approximately 30% faster than silicon, while 4H-SiC demonstrates an electron mobility of 950 cm²/V-s. These disparities play a crucial
role in defining the advantages offered by each technology in specific power levels and target applications. The superior electron mobility of GaN renders it highly suitable for high-performance and high-frequency applications [5], [11]-[14]. On the other hand, 4H-SiC, with its higher thermal conductivity and lower frequency operation, is better suited for high-power applications that necessitate elevated voltage levels. This includes various domains such as electric vehicles (EVs), data centers, solar power designs, rail traction, wind turbines, grid distribution, and industrial and medical imaging. Although high-frequency switching is not always a requirement in these applications, the higher-voltage operation and improved heat dissipation properties of 4H-SiC prove advantageous [8]-[10], [13], [14]. It is evident that both GaN and 4H-SiC outperform traditional silicon in power processing and fast charging. GaN with voltage levels 650V offers faster switching, integration, and reduced costs, making it well-optimized for applications up to 20kW. On the other hand, 4H-SiC excels in higher voltage ranges, specifically for devices exceeding 1000V, and is ideal for applications up to 20MW, capitalizing on its enhanced voltage and temperature capabilities [13], [14].

Silicon carbide (4H-SiC) power devices have undergone a significant commercialization journey over the past decades. Fig. 1.2 shows some of the key 4H-SiC developmental milestones over the years [15]. The exploration of 4H-SiC as a semiconductor material for power devices began in the 1980s. Early research focused on material growth techniques, device design, and fabrication processes to harness the unique properties of 4H-SiC [16]. By the early 2000s, 4H-SiC power devices began to enter the market, primarily targeting niche applications that required the unique capabilities of 4H-SiC, such as high-power inverters, hybrid electric vehicles (HEVs), and renewable energy systems. These early commercial products paved the way for wider adoption and demonstrated the reliability and performance benefits of 4H-SiC devices. In the following
years, advancements in 4H-SiC material quality, device design, and manufacturing processes led to improved device performance, higher voltage ratings, and increased product availability.

**Figure 1.2: 4H-SiC developmental milestones [15], [16]**

By the early 2000’s the demand for 4H-SiC power devices is on the rise due to their superior performance and efficiency compared to traditional silicon-based devices. The increasing adoption of 4H-SiC devices can be attributed to their benefits in terms of higher switching frequencies, reduced power losses, and improved system efficiency. 4H-SiC power devices find applications in various sectors, including automotive, industrial, renewable energy, and aerospace. In automotive applications, 4H-SiC devices are used in EV powertrains, on-board chargers, and DC-DC converters, offering advantages such as higher efficiency, faster switching, and compact system design. Industrial applications include motor drives, power supplies, and UPS systems, where 4H-SiC devices provide improved power density and energy efficiency. The market for 4H-SiC power devices is witnessing expansion as more manufacturers enter this space. Established semiconductor companies, as well as emerging players, are investing in 4H-SiC technology to
capitalize on its growth potential. This increased competition is expected to drive technological advancements, cost reductions, and further market expansion [15]-[23].

Over the last decade, as 4H-SiC power devices transition from niche to mainstream applications, there is a growing focus on mass production and cost reduction. Manufacturers (Mitsubishi, OnSemi, ROHM, Wolfspeed, Infineon, and ST Micro) are investing in larger wafer sizes, advanced fabrication processes, and economies of scale to achieve cost competitiveness and meet the increasing demand for 4H-SiC devices [15]-[23].

The significant strides made in mass adoption, commercialization, and the widespread understanding of material properties, along with advancements in design and manufacturing processes of the discrete 4H-SiC devices have set the stage for the next phase of technological advancement: “The Development of Power ICs in 4H-SiC”. Similar to the trajectory of many pioneering technologies that originate from academic research, the inception of HV Power ICs in 4H-SiC, specifically known as SMART Power ICs, also originated with this project. The exceptional advancements and the significant progress that was made are reported in this dissertation.

1.2 Development of SMART 4H-SiC Power ICs

1.2.1 Introduction to Power ICs

Power IC technology refers to the integration of power management functions and control circuitry into a single integrated circuit [24]-[26]. Power ICs utilize various types of power devices, including metal-oxide-semiconductor field-effect transistors (MOSFETs), bipolar junction transistors (BJTs), insulated-gate bipolar transistors (IGBTs), and diodes [24]-[26]. These devices
are integrated with control circuitry, such as voltage regulators, gate drivers, and protection circuits, on a single chip enabling efficient power conversion, regulation, and management. Power ICs are designed to handle high currents and voltages, making them suitable for various applications in industries such as consumer electronics, automotive, industrial, and renewable energy systems [24]-[26]. A typical pictorial representation of a power IC (layout components from this work) is shown in Fig. 1.3.

![4H-SiC 600V Lateral Power MOSFET, 4H-SiC CMOS control circuitry, 4H-SiC Integrated Power IC](images.png)

**Figure 1.3:** Pictorial representation of Power MOSFET, CMOS, and Integrated Power IC in 4H-SiC (Images from this project)

The integration of power functions within a single IC offers significant advantages. Primarily, it reduces the overall size and complexity of the system, enabling miniaturization and saving overall footprint [24]-[26]. Additionally, power ICs provide improved performance, higher energy efficiency, and enhanced reliability compared to discrete power components. By integrating power devices and control circuitry, power ICs can achieve better matching and synchronization between the power stage and control signals, resulting in optimized system performance [24]-[34].
1.2.2 Motivation for 4H-SiC Power IC technology

The current generation power IC (multiple power integrated functions onto a single chip) technologies, predominantly Bulk Silicon and Silicon-On-Insulator (SOI) technologies have limitations in their operational temperatures and power handling capability [36]. Any temperatures beyond the standard commercial temperature (0 °C to +85 °C) or the military specification temperature standard (−55 °C to +125 °C) are considered extreme/high temperatures [37]. Based on the theoretical limits, Si-based ICs are rated at 150 °C and are not operational beyond 200 °C due to leakage and reliability issues. Although SOI technology offers relief up to 300 °C, with the insulated region, it also fails beyond 300 °C [36]. For the past few decades, 4H-SiC has been a reliable material for the development of high-voltage and high-temperature power devices. Due to its superior material properties, 4H-SiC power devices can operate at high power and high temperatures when compared to their Si counterparts [38]-[40]. In the present-day context, Si-based power and control ICs are responsible for driving HV discrete 4H-SiC MOSFETs. However, this technology leads to an increase in the system's size and introduces parasitic effects from interconnects, which negatively impacts reliability. Moreover, the advantageous high-temperature operation of 4H-SiC remains untapped. To overcome these challenges and address the high power and extreme temperature issues associated with Si power ICs, a viable solution emerges the integration of the HV Power MOSFET with LV CMOS on a single 4H-SiC-based IC. This monolithic integration can significantly enhance performance and reliability. The progress achieved in material development and device fabrication over the past decade has made the seamless development of 4H-SiC-based PICs (Power Integrated Circuits) possible. This breakthrough opens up new opportunities for power electronics, paving the way for more efficient and robust systems.
Considering the current state of maturity and economic feasibility, it is improbable that 4H-SiC-based power ICs would offer significant benefits at temperatures below 300 °C when compared to Bulk Si and SOI technologies. However, notable advancements in device design have allowed Bulk Si and SOI-based LDMOS technology to achieve blocking voltages up to 800V. Despite this achievement, the $R_{on,sp}$ of the Silicon lateral devices [41]-[45] remain higher than 4H-SiC-based lateral MOSFETs [46]-[54]. Consequently, even at temperatures below 300°C, 4H-SiC power ICs can prove to be a viable solution in scenarios where higher power levels are required. However, as the temperature surpasses the 300°C threshold, the author acknowledges that 4H-SiC-based power ICs hold incredible potential to serve as a promising solution for the development of high-power and high-temperature ICs.

1.2.3 4H-SiC HV Lateral MOSFET — its significance and potential

The distinctive factor distinguishing lateral and vertical MOSFETs lies in their specific on-resistance ($R_{on,sp}$). In the case of lateral MOSFETs, the primary contributors to resistance are channel and drift resistances. To gain insights into these resistance components in both lateral and vertical MOSFETs, a comprehensive study was conducted, as depicted in Fig. 1.4. The calculations were based on reasonable assumptions and well-established specifications, which are summarized in Fig. 1.4’s description.

Figure 1.4a illustrates that, for voltage ratings below 200V, lateral MOSFETs exhibit lower specific on-resistance compared to their vertical counterparts. However, a noteworthy observation arises when channel mobility is increased to 50 and 100 cm$^2$/V-s, as shown in Figures 1.4b and 1.4c. In these scenarios, the dominance of lateral MOSFETs extends to the 700V and approximately 900V ranges, respectively.
Assumptions for calculations:

tox = 50 nm (SiO₂)
Channel length = 0.5 μm
Lateral device blocking capability = 200V/μm
Gate Voltage = 25V
Threshold voltage = 3V
Substrate thickness and resistivity: 350μm; 20mΩ-cm
This highlights the significance of channel mobility as a primary contributor to resistance, indicating that any enhancement in channel mobility leads to a substantial reduction in the overall resistance of lateral MOSFETs. The 4H-SiC community has been engaged in relentless endeavors aimed at enhancing channel mobility in 4H-SiC. Over the years, significant advancements have been made to unravel the intricacies associated with channel mobility [55]-[61]. These diligent efforts will pave the breakthrough which will further enhance the performance of the 4H-SiC power devices.

The validation of these calculations is further supported by our experimental development of a 600V 4H-SiC HV lateral MOSFET [5], which confirms that the channel resistance plays a dominant role in the total specific on-resistance of the lateral device. This comprehensive evaluation not only demonstrates the potential of 4H-SiC lateral MOSFETs in voltage ranges below 1.2kV but also establishes their suitability for power IC development, particularly requiring power MOSFETs operating in the 400V-800V range. These findings underscore the favorable characteristics of 4H-SiC lateral MOSFETs and their applicability in power ICs, paving the way for advancements in high-performance and efficient power electronic systems.

### 1.2.4 Power IC integration technologies

The type of HV MOSFET architecture plays a crucial role in defining the application space for Power ICs. At present, only a limited number of research groups, including our own, have reported the integration of HV MOSFETs with CMOS technology in 4H-SiC for Power IC development. In the research conducted at SUNY, successful integration of Lateral HV MOSFETs with LV CMOS was achieved, as demonstrated in Fig. 1.5 [52]. As part of ongoing research and development efforts, integrating HV Vertical MOSFETs with CMOS is being explored, employing
the same process technology. The cross-section of the Vertical MOSFET-integrated CMOS structure is illustrated in Fig. 1.6. Additionally, another research group at AIST [62] has dedicated its efforts to integrating HV Vertical MOSFETs with LV CMOS, as depicted in Fig. 1.7. These endeavors aim to expand the range of possibilities for Power ICs and drive advancements in the field of HV MOSFET integration with CMOS technology.

**Figure 1.5:** Cross-section showing the monolithic integration of the HV lateral MOSFET, LV NMOS, and LV PMOS on an N-epi, P-epi grown on N+ substrate [52]

To gain a comprehensive understanding of both integration technology platforms, a study has been conducted, encompassing various aspects of the integration process. The key insights from this contemplation are summarized in Table 1.2, providing a valuable reference for researchers and engineers working in the field of HV MOSFET integration for Power IC applications. These comparative analyses enable a better understanding of the strengths and limitations of each integration approach.
Figure 1.6: Cross-section showing the monolithic integration of the HV vertical MOSFET, LV NMOS, and LV PMOS on an N-epi grown on an N+ substrate

Figure 1.7: Cross-section showing the integration of the HV vertical MOSFET, LV NMOS, and LV PMOS on a P-epi, N-epi grown on an N+ substrate[62]
<table>
<thead>
<tr>
<th>Feature</th>
<th>HV lateral MOSFET + CMOS</th>
<th>HV vertical MOSFET + CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power MOSFET architecture</strong></td>
<td>Lateral</td>
<td>Vertical</td>
</tr>
<tr>
<td><strong>Low voltage technology</strong></td>
<td>CMOS</td>
<td>CMOS</td>
</tr>
<tr>
<td><strong>Epi stack</strong></td>
<td>N-epi/P-epi/ N+ Substrate</td>
<td>N-epi/N+ Substrate or P-epi/N-epi/N+ Substrate</td>
</tr>
<tr>
<td><strong>Pursuit of Half-bridge Power IC – Critical building block in the field of power electronics</strong></td>
<td>Integration of multiple power MOSFETs with no constraints is one of the significant advantages of this technology. This integration opens tremendous scope for implementing various power electronic circuit architectures</td>
<td>Due to the vertical architecture, multiple power MOSFETs that operate at different states (High-side and Low-side) cannot be integrated. This is a major drawback that limits the level of system integration in this technology</td>
</tr>
<tr>
<td><strong>Power rating</strong></td>
<td>High blocking voltage (&gt;1200V) requires a large footprint which might compromise the performance</td>
<td>Possible to achieve high blocking voltages and allows to extract large densities of current</td>
</tr>
<tr>
<td><strong>Electromagnetic Noise-induced from the Power MOSFET</strong></td>
<td>Minimal since the lateral power MOSFET is isolated from the microelectronic CMOS</td>
<td>The CMOS circuitry is prone to noise due to the vertical architecture of the power MOSFET</td>
</tr>
<tr>
<td><strong>Process complexity</strong></td>
<td>Simple process flow similar to the well-established 4H-4H-SiC discrete planar MOSFETs</td>
<td>N-epi/N+ Substrate — Simple process flow similar to the well-established 4H-4H-SiC discrete planar MOSFETs P-epi/N-epi/N+ Substrate — Complicated process involving epi-regrowth and trench formation</td>
</tr>
</tbody>
</table>
Analyzing the data presented in Table 1.2 reveals that both integration technologies have their advantages and disadvantages at different voltage ratings. However, given the current stage of development and the lack of clear consensus in the field, it would be premature and misleading to assert that one integration technology surpasses the other in terms of performance and economic considerations. The immaturity and ambiguity surrounding these technologies necessitate further investigation and comparative analysis before definitive conclusions can be drawn regarding their superiority or suitability for specific applications. Continued research and development efforts are vital for enhancing our understanding of these integration technologies and unlocking their full potential in the context of performance and economic viability.

1.2.5 Approach for development of SMART ICs

Supported by ARPA-E funding [63], a collaborative team consisting of SUNY Polytechnic Institute, Ohio State University, and North Carolina State University embarked on a research initiative to advance the development of scalable, manufacturable, and robust technology for 4H-SiC power integrated circuits known as SMART 4H-SiC Power ICs. To realize this goal, disruptive device designs, architectures, and processes, via novel gate oxide and CMOS technology, were developed to monolithically integrate the HV lateral power MOSFETs (400 V – 600 V rated) with 4H-SiC LV CMOS and on 100/150 mm 4H-SiC substrates and thereby demonstrating the operation of HV Power ICs. Fig. 1.8 captures the strategy employed to establish the SMART IC technology platform. Extensive 2D Synopsis device and process simulations have been used to optimize the novel device (cell and peripheral) design architectures ensuring optimal performance to be implemented within the Power IC. Critical process module developments, and implant recipes have been designed in close collaboration with the ADI Hillview fabrication facility in San Jose,
CA, and SiCamore Semi in Bend, OR, to establish the process technology platform. Industry-standard packaging efforts have been employed to characterize the designed HV and HT 4H-SiC ICs. Within this collaborative effort, SUNY took the lead in design and process development, with OSU and NCSU making significant contributions to IC design implementation and gate oxide recipe development, respectively. This dissertation encompasses the comprehensive endeavors undertaken at SUNY to drive the development of SMART Power ICs throughout the project's duration, providing valuable insights into the various stages of design, fabrication, and process optimization.

Figure 1.8: Framework employed to establish a SMART 4H-SiC Power IC platform
Fig. 1.9 shows the technology road map of this project. As an initial stride in achieving that landmark goal of this project, in Lot 1, the HV Lateral MOSFET and LV CMOS are monolithically integrated on a 6-inch N-epi on N+ substrate using a single process flow [51]. Although in Lot 1, the HV and LV components are monolithically integrated, they all share the same conducting N+ substrate thereby lacking the isolation which is a significant requisite in developing HV Power ICs on a single chip. Accordingly, moving one step forward, the epi stack has been modified and optimized to N-epi/P-epi/N+ substrate such that the LV blocks (CMOS control circuitry) are completely isolated yet integrated with the HV Lateral MOSFET as shown in Fig. 1.5 [52]. P+ isolation in conjunction with P-epi is used to isolate the LV from HV blocks. Similar to Lot 1, a single gate oxide and ohmic process are used to integrate the HV and LV CMOS devices. Also, in Lot 2 an advanced back-end-of-the-line (BEOL) process with three metal layers was employed, offering an edge in flexible metal routings and in developing scalable Power ICs. Based on the learning from Lot 1 and Lot 2, Lot 3 and Lot 4 have been designed and are currently being fabricated to demonstrate an Isolated and non-isolated buck converter and Half-bridge power driver IC respectively.

Notably, in Lot 3 a novel HV lateral MOSFET architecture (Gen 2) has been demonstrated [64] that addresses the prominent surface field challenges commonly encountered in lateral MOSFET designs. The gate-channel-JFET areas of the Gen 2 design bear a striking resemblance to those of popular 4H-SiC vertical MOSFETs, which enables the application of similar techniques to enhance field management, reliability, and ruggedness. Consequently, this innovative architecture presents a highly promising solution that presents an excellent solution for the design of lateral MOSFETs.
Figure 1.9: Technology roadmap outlining the progression for the development of SMART Power IC; the goals and accomplishments of each lot are summarized

1.3 Outline

This dissertation presents the design and development of SMART Power ICs in silicon carbide (4H-SiC). Before the dedicated chapters on SMART Power IC development, Chapter 2 provides an in-depth exploration of drift layer design and presents a comprehensive trade-off analysis specifically for 4H-SiC and other wide bandgap semiconductors. The analysis encompasses critical factors such as breakdown voltage assessment based on impact ionization coefficients, the consequential dependence of critical electric field on doping concentration, and the importance of incomplete ionization for specific on-resistance considerations. The insights gained from this section empower researchers to make informed decisions when optimizing the NPT and PT drift layer designs for wide bandgap semiconductors. Additionally, the drift layer design for unipolar power devices within the voltage range of 600V to 25kV, with particular
emphasis on 4H-SiC was reported. Both NPT and PT (Punch-Through) designs are explored, and mathematical power series curve fitting techniques are employed to derive simplified generalized equations tailored to NPT and PT designs. These equations serve as invaluable design guidelines, offering valuable insights into appropriate drift layer architectures based on the desired voltage rating.

Chapter 3 focuses on providing a process document that serves as a guide for design and fabrication teams, enabling them to complete a full manufacturing run of SMART 4H-SiC Power IC technology. It highlights key considerations such as starting materials, fabrication process flow, device designs, and high-voltage and low-voltage integration. This chapter also equips designers with valuable simulated and experimental information on the fabricated components to ensure successful design outcomes.

Chapter 4 focuses on the development of high-voltage lateral Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and diodes in 4H-SiC, specifically tailored for integration within power ICs. The comprehensive development process includes simulations and in-depth analysis of experimental results for these devices. The initial phase of high-voltage (HV) device development involves experimentation on an N-epi/N+ substrate, followed by successful implementation on the N-epi/P-epi/N+ substrate for the Power ICs. The outcome of these lateral device developments is superior BV-R_{on,sp} trade-off performance in their class (400V-600V). Another highlight of this work is a novel architecture (Gen 2) with a highly reliable and robust design addressing the prominent field management issues in lateral devices.

Chapter 5 addresses the need for high voltage isolation in power IC technology to ensure the safety, reliability, and proper functioning of electronic systems. Various high-voltage isolation techniques to prevent electrical leakage and isolate sensitive circuitry from potentially damaging voltage
levels are discussed. The use of junction isolation, specifically the P+ Isolation junction implemented by channeling implantation, is highlighted, with its design and effectiveness supported by electrical measurements. Additionally, the interlayer dielectric (ILD) voltage-blocking capability for metal-to-metal insulation between adjacent metal layers carrying different voltage potentials is addressed. Measurements are performed to evaluate the ILD blocking capabilities between metals, such as Metal 1 to Metal 2 and Metal 2 to Metal 3.

Chapter 6 presents an extensive study on peripheral and edge termination techniques for lateral power devices. Using 2D TCAD simulations, techniques are designed at the edges of lateral devices to control and distribute the electric field, thereby improving breakdown voltage and ensuring reliable operation. The significance of layout techniques is discussed, highlighting how lateral device layout techniques eliminate the need for edge termination while still offering similar static performances as the ones with edge termination. Additionally, a summary table is provided, capturing performance metrics, chip sizes, and power IC feasibility.

Chapter 7 reports on the results and discusses the design of module processes implemented for complementary metal-oxide-semiconductor (CMOS) development. Channel engineering techniques are applied to good designs with accumulation and inversion mode channels. Multiple gate oxide recipes are developed to simultaneously target the maximum possible channel mobilities of electrons and holes. Efforts are dedicated to improving CMOS performance through optimized ohmic contacts, including the pursuit of metal contacts for the simultaneous formation of n-type and p-type ohmic contacts.

Chapter 8 explores the potential scope for high-temperature (HT) integrated circuits (ICs) in 4H-4H-SiC through a literature survey. Building upon the CMOS technology efforts discussed in Chapter 7, the chapter demonstrates the performance of CMOS ICs to justify the potential of the
developed technology. The chapter also evaluates the operation of digital CMOS ICs at extreme temperatures up to 400°C, covering packaging flow, assembly process, materials employed, and challenges encountered during HT measurements of the ICs. Although the ultimate objective of this work is to develop 4H-SiC-based high-voltage (HV) power ICs, this chapter focuses on evaluating the operation of CMOS ICs at extreme temperatures to assess their suitability.

1.4 References


S. B. Isukapati *et al.*, “Monolithic Integration of Lateral HV Power MOSFET with LV CMOS for SiC Power IC Technology,” in *2021 33rd International Symposium on Power*


CHAPTER 2: Drift Layer Design and Trade-off Analysis in 4H-SiC and Other Wide Bandgap Semiconductors

2.1 Introduction

The drift layer design plays a crucial role in the performance and functionality of power semiconductor devices. It directly impacts the voltage-blocking capability, on-state resistance, switching characteristics, breakdown voltage uniformity, and long-term reliability of the devices [1]-[3]. By carefully designing the drift layer’s doping concentration, thickness, and material properties, engineers can optimize the device's ability to withstand high voltages, minimize conduction losses, achieve fast switching speeds and ensure uniform voltage distribution. The drift layer design is a critical aspect that enables the development of efficient and high-performance power semiconductor devices, enabling their use in various applications, ranging from power transmission systems to electric vehicles, and renewable energy systems. The examination of 1D limitations proves to be particularly advantageous in comprehending the fundamental behavior and characteristics of these emerging wide bandgap materials which aid in formulating their technological trajectories.

This chapter delves into the design of the drift layer and presents a comprehensive trade-off analysis for 4H-SiC and other wide bandgap semiconductors. The chapter is organized into three main sections, each addressing specific aspects of the drift layer design.

Sections 2.2 to 2.6 focus on the physics of the P+/N-/N+ diode, including the phenomenon of impact ionization and the calculation of the ionization integral. Then a step-by-step design flow for designing the drift layer of an abrupt P+/N-/N+ junction diode is shown in the form of a flow
chart (section 2.7). This lays the groundwork for understanding the principles behind drift layer design in wide bandgap semiconductors.

In section 2.8, the discussion revolves around one specific configuration of the drift layer known as non-punch-through (NPT). The trade-off relationships for various wide bandgap semiconductors are thoroughly evaluated in this context. The analysis takes into account factors such as evaluating the breakdown voltage from impact ionization coefficients and as a result critical electric field dependence on doping concentration, incomplete ionization essential for specific on-resistance, enabling researchers to make informed decisions when optimizing the NPT drift layer design for wide bandgap semiconductors.

Section 2.9 discusses the conflicting impact ionization coefficients and their corresponding trade-offs in Diamond letting the designers know the criticality of meticulous scrutiny and cautious selection of impact ionization coefficients from the existing literature to ensure accurate assessment and optimization of trade-off performance parameters.

Section 2.10 focuses exclusively with an emphasis on drift layer design for unipolar power devices (600V to 25kV) in 4H-SiC. In this section, considerations for both NPT and PT designs are explored. Furthermore, mathematical power series curve fitting techniques are employed to derive simplified generalized equations for NPT and PT designs. These equations serve as valuable design guidelines for device researchers, offering insights into the appropriate drift layer architectures based on the desired voltage rating.

In the concluding part, section 2.11 briefly touches upon the dynamic performance disparity concerning NPT versus PT drift layer designs.
2.2 Abrupt PN Junction

Power devices are specifically designed to withstand high voltages through the utilization of a depletion layer formed at various interfaces, such as P-N junctions, metal-semiconductor (Schottky barrier) contacts, and metal-oxide-semiconductor (MOS) interfaces [1]-[3]. This investigation focuses on analyzing the design aspects of non-punch-through (NPT) and punch-through (PT) within the context of a PN junction.

![Diagram of PN Junction](image)

**Figure 2.1**: Typical triangular electric field profile for an NPT design; the slope of the electric field pattern denotes the doping concentration, and the area of the electric field pattern represents the breakdown voltage.

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2.3 Triangular-shaped electric field profile (Non-Punch Through)

In the reverse-biased state, where a positive voltage is applied to the N+ side (Cathode), a significant electric field is generated, leading to the expansion of the depletion region towards the N-epi/drift and the electric field goes to zero at the N-/N+ junction, resulting in a triangular shape of the electric field as shown in Fig. 2.1. During the device's blocking mode of operation, the depletion region on the P+ side remains minimal due to the high doping of the P+ region. By effectively extending the depletion region, the device can withstand high voltages without experiencing a breakdown. This depletion layer acts as a barrier to prevent excessive current flow, ensuring the device operates within its intended blocking mode. The slope of the electric field pattern denotes the doping concentration, and the area of the electric field pattern represents the breakdown voltage. This type of design configuration is called Non-Punch-Through (NPT).

By integrating the Poisson’s equation for N- the region with the boundary condition that the electric field goes to zero at the edge of the depletion region (width of depletion = W_{NPT}) gives the electric field distribution [1], [2] as

\[ E(x) = \frac{qN_{D,NPT}}{\varepsilon} (W_{NPT} - x) \]  

By evaluating the potential distribution through the N- region and applying the boundary conditions, the width of the depletion is given by (2)

\[ W_{NPT} = \sqrt{\frac{2\varepsilon BV}{qN_{D,NPT}}} \]  

2.4 Trapezoidal-shaped electric field profile (Punch-Through)

On the other hand, the design is called Punch-Through (PT) when a thinner drift layer is adopted, while reducing the doping concentration to achieve the same breakdown voltage as the NPT structure \( (A_1 = A_2) \) as shown in Fig. 2.2. The PT design forms a trapezoidal shaped electric field profile at the breakdown as shown in Fig. 2.2.

![Trapezoidal electric field profile](image)

**Figure 2.2:** Typical trapezoidal electric field profile for a PT design; the area of the electric field pattern represents the breakdown voltage

Due to the trapezoidal-shaped electric field profile, considering the additional electric field at the N-epi / N+ region and also the voltage supported across the PT, the electric field of the PT at the onset of BV is given by (3)
\[ E(x) = \frac{1}{W_{D,PT}} \left( BV + \frac{(qN_{D,PT}(W_{D,PT} - x)^2)}{2\varepsilon} \right) \] (3)

### 2.5 Impact ionization and ionization integral

Impact ionization is a phenomenon that occurs in semiconductor devices when carriers (electrons or holes) gain sufficient energy from the electric field, leading to the creation of electron-hole pairs through collision processes. The generated electron-hole pairs are then accelerated by the electric field, leading to a multiplication effect as these carriers gain enough energy to cause further ionization events. This positive feedback loop results in an avalanche breakdown, where the device's current increases rapidly [1]-[3].

Impact ionization coefficients which are defined as the number of e-h pairs created by a carrier before traveling 1cm through depletion of various wide bandgap semiconductors are given in Chynoweth’s form [4] as

\[ \alpha_n = a_n e^{\left(\frac{-b_n}{E(x)}\right)^{m_n}} \quad (4) \]

\[ \alpha_p = a_p e^{\left(\frac{-b_p}{E(x)}\right)^{m_p}} \quad (5) \]

Multiple research groups have extensively investigated the impact ionization coefficients of wide bandgap semiconductors [5]-[19], yielding a plethora of reported values. However, due to variations in the maturity level of these semiconductor materials, a significant disparity exists among the reported impact ionization coefficients. The selection of appropriate impact ionization coefficients plays a pivotal role in conducting trade-off analyses accurately. The performance trade-offs are directly influenced by the choice of impact ionization coefficients, which, in turn, are contingent upon factors such as material quality, device design, and the effectiveness of edge
termination techniques. Therefore, the authors of this study acknowledge the criticality of meticulous scrutiny and cautious selection of impact ionization coefficients from the existing literature to ensure accurate assessment and optimization of trade-off performance parameters. Fig. 2.3 shows the widely used impact ionization coefficients of 4H-SiC [7], GaN [10], Ga2O3 [13], and Diamond [16] as a function of the electric field at 25 °C.

![Impact ionization coefficients graph]

**Figure 2.3:** Impact ionization coefficients of various wide bandgap semiconductors at 25 °C

The ionization integral is a key parameter used to determine the breakdown voltage of power devices. It quantifies the impact ionization process that occurs within the semiconductor material under high electric field conditions, leading to the generation of electron-hole pairs and eventual breakdown. The ionization integral provides a means to calculate and analyze the impact ionization process, aiding in the prediction and understanding of breakdown behavior. The ionization integral is typically obtained through experimental measurements or numerical simulations.
Solving the ionization integral involves integrating the impact ionization coefficient, which characterizes the rate at which electron-hole pairs are generated, concerning the electric field strength across the device. By evaluating the ionization integral (6), insights into the breakdown behavior and voltage-blocking capabilities can be evaluated. Semiconductor materials like Si, 4H-SiC, and GaN have well-documented solutions of ionization integrals, which describe the impact ionization process and breakdown behavior in these materials. However, when it comes to more recent wide bandgap semiconductor materials, the understanding of multiplication and breakdown characteristics is limited. This work focuses on addressing this knowledge gap by analyzing the multiplication and breakdown properties of these emerging wide bandgap semiconductor materials. The ionization integral should be solved numerically using several mathematical techniques (Gauss quadrature, bisection, trapezoidal rule, etc.) where the values are iteratively varied until the integral converges to 1.

\[ \int_{0}^{W_D} \alpha_p e^{(-I_0^x(\alpha_p-\alpha_n)dx')} dx = 1 \quad (6) \]

*Note: Gauss quadrature numerical integration method is used to evaluate the ionization integral in this analysis*

### 2.6 Incomplete ionization in wide bandgap semiconductors

The role of incomplete ionization is crucial in evaluating the specific on-resistance \((R_{on,sp})\) of the drift layer. The specific on-resistance represents the resistance encountered by current flow in the conducting state, normalized by the device area. It is a key parameter used to assess the semiconductor’s efficiency and performance. Incomplete ionization refers to the phenomenon where not all dopant atoms in the semiconductor material contribute to the generation of charge
carriers (electrons or holes). This occurs when the dopant atoms are not fully ionized, meaning they do not release their full complement of free carriers into the conduction or valence bands. When the dopant atoms are not fully ionized, the available carriers for conduction are reduced, leading to higher resistance, and increased specific on-resistance. The level of incomplete ionization depends on various factors, such as doping concentration, material properties, and temperature. Higher doping concentrations or lower temperatures can increase the degree of incomplete ionization and, consequently, raise the specific on-resistance.

Hence it is mandatory that the carrier density \( N_{D,NPT}^+ \) is used to accurately evaluate the specific on-resistance and not the doping density \( N_{D,NPT} \). The specific on-resistance of the NPT drift layer with thickness of \( W_{NPT} \) is given by (7).

\[
R_{sp,NPT} = \frac{W_{NPT}}{q\mu_n N_{D,NPT}^+} [\Omega \cdot \text{cm}^2] \quad (7)
\]

The accurate evaluation of incomplete ionization in this work involved determining the energy levels of donors and acceptors for each dopant in the semiconductor material. To accomplish this, extensive research has been conducted to obtain and analyze the ionization energy levels of dopants in different semiconductors. The ionization energy levels of various semiconductor materials, as reported in the literature, are summarized in Table 2.1.

In evaluating the ionization ratios of donors and acceptors in semiconductor materials, a degeneracy factor of 2 and 4 is typically considered for donors and acceptors, respectively \([2]\). For 4H-SiC, GaN, and Ga\(_2\)O\(_3\) n-type dopants, and diamond, the p-type dopant is prominently used to design the drift layers. Fig. 2.4 shows the ionization fractions for Nitrogen donors in 4H-SiC, Silicon donors in GaN, Tin donors in Ga\(_2\)O\(_3\), and Boron acceptors for diamond evaluated at 25°C. It is observed that Diamond, characterized by large ionization energies, exhibits remarkably low
ionized acceptors across the doping range. Consequently, this phenomenon contributes to a significant increase in the specific on-resistance of Diamond-based devices as shown in Fig. 2.10.

Table 2.1: Ionization energy levels of various semiconductor materials

<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>Donors</th>
<th>Acceptors</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dopant</td>
<td>Donor energy level (meV)</td>
</tr>
<tr>
<td>Ga2O3</td>
<td>Tin</td>
<td>30 [26]</td>
</tr>
</tbody>
</table>

Figure 2.4: Ionization fraction for donors in 4H-SiC, GaN, Ga2O3 and acceptors for diamond semiconductor materials at 25°C
2.7 Comprehensive flowchart outlining drift design

Figure 2.5 illustrates a comprehensive flowchart outlining the drift layer design methodology for any semiconductor material, whether it follows the non-punch-through (NPT) or punch-through (PT) design approach. The design process begins by obtaining the impact ionization coefficients of electrons and holes specific to the semiconductor material under consideration. In the NPT design, the objective is to achieve a desired breakdown voltage (BV) for which there exists a unique set of parameters: \( N_{D,NPT} \) region) and \( W_{D,NPT} \). To determine this unique combination, an iterative process is employed. The \( N_D \) value is adjusted iteratively until the ionization integral reaches unity, indicating the desired BV has been achieved. Once the \( N_{D,NPT} \) is determined, the corresponding values for \( W_{D,NPT} \) and \( E_{c,NPT} \) are extracted. These parameters are critical for the NPT drift layer design. Finally, using the obtained values for \( W_{D,NPT} \), \( E_{c,NPT} \), and \( N_{D,NPT} \), the specific on-resistance (\( R_{on,sp} \)) associated with the NPT design can be calculated.

In the context of PT design, the complexity arises from the trapezoidal shape of the electric field, making mathematical computations challenging. When targeting a specific BV, there exist numerous combinations of \( W_{D,PT} \) and \( N_{D,PT} \) that can achieve the desired BV. To solve the ionization integral for a specific BV, a systematic variation of the doping concentration in the drift layer was performed while maintaining a constant \( W_{D,PT} \). Calculations were performed to evaluate the drift resistance and breakdown voltage for a range of PT structures. This comprehensive calculation approach enabled the exploration of different combinations of drift layer thickness and doping density, covering a wide parameter space. To determine the optimal point on this trade-off curve, which corresponded to the lowest drift resistance achievable at a specified breakdown voltage, a trade-off relationship between drift resistance and breakdown voltage should be established as outlined in Fig. 2.5.
Figure 2.5: Flowchart showing the drift layer design methodology either by NPT or PT from impact ionization coefficients.
2.8 BV – $R_{on,sp}$ trade-off of 4H-SiC and other wide bandgap semiconductors

Based on the impact ionization coefficients and abiding by the methodology outlined for NPT design in Fig. 2.5, the BV-$R_{on,sp}$ trade-off for 4H-SiC and other wide bandgap semiconductors have been evaluated in this section.

Figure 2.6: Critical field for avalanche breakdown in a 4H-SiC and other wide bandgap semiconductors in 25°C

Fig. 2.6 shows the critical electric field strength dependence as a function of doping density. As observed, Gallium oxide has the largest critical electric field strength across the doping ranges when compared to other wide bandgap semiconductors. The critical field in 4H-SiC at 25°C was approximated using an empirical expression by Konstantinov [7] and the same was done for other wide bandgap semiconductors in equations (9), (10), and (11).
\[ E_{c(SiC)} = \frac{2.49 \times 10^6}{1 - 0.25 \log_{10} \frac{N_{D,NPT} (cm^{-3})}{10^{16}}} \]  \[ 7 \] \[ \text{(8)} \]

\[ E_{c(GaN)} = \frac{3.29 \times 10^6}{1 - 0.35 \log_{10} \frac{N_{D,NPT} (cm^{-3})}{10^{16}}} \] \[ \text{(9)} \]

\[ E_{c(Ga_2O_3)} = \frac{5.25 \times 10^6}{1 - 0.285 \log_{10} \frac{N_{D,NPT} (cm^{-3})}{10^{16}}} \] \[ \text{(10)} \]

\[ E_{c(Diamond)} = \frac{1.60 \times 10^6}{1 - 0.5 \log_{10} \frac{N_{D,NPT} (cm^{-3})}{10^{16}}} \] \[ \text{(11)} \]

**Figure 2.7:** Doping density of the NPT drift layer versus the breakdown voltage in 4H-SiC and other wide bandgap semiconductors
Figs. 2.7 and 2.8 show the doping density and width of the drift layer versus breakdown voltage for the NPT structures in 4H-SiC and other wide bandgap semiconductor unipolar devices. As outlined in section 2.7, the doping density and width for the NPT structure can be uniquely determined for each voltage.

**Figure 2.8:** Width of the NPT drift layer versus the breakdown voltage in 4H-SiC and other wide bandgap semiconductors

The specific on-resistance of the NPT drift layer with a thickness of $W_{NPT}$ is given by (12). In line with the discussion in section 2.6, it is crucial to utilize the carrier density ($N_{D,NPT}^+$) rather than the doping density ($N_{D,NPT}$) for precise evaluation of $R_{on,sp,NPT}$. Additionally, when considering incomplete ionization effects, it is essential to account for the dependence of mobility on doping density. This consideration ensures an accurate assessment of the specific on-resistance by incorporating both incomplete ionization effects and the influence of mobility on doping dependence.
Figure 2.9: Mobility dependence on doping concentration for 4H-SiC [27], GaN [28], Ga2O3 [29], and diamond [30] at 25°C

Figure 2.10: Trade-off relationship between the specific on-resistance and breakdown voltage in 4H-SiC, GaN, Ga2O3, and Diamond at 25°C; the trade-off plot of Silicon was also added
\[ R_{\text{sp,NPT}} = \frac{W_{\text{NPT}}}{q\mu_n N_{\text{D,NPT}}} [\Omega \cdot \text{cm}^2] \]  (12)

Fig. 2.9 shows the mobility dependence on the doping concentration for 4H-SiC [27], GaN [28], Ga2O3 [29], and diamond semiconductors [30] at 25°C. Fig. 2.10 presents a comprehensive analysis of the trade-off relationship between specific on-resistance and breakdown voltage across four wide bandgap semiconductors: 4H-SiC, GaN, Ga2O3, and Diamond. In contrast, Fig. 2.11 displays the ideal trade-off plot for these wide bandgap semiconductors. However, it is essential to acknowledge that certain approximations have been made in the evaluation process of Fig. 2.11, including assuming a constant critical electric field, maintaining constant mobility across the doping range, and neglecting the influence of incomplete ionization of donors or acceptors. These approximations can lead to an overestimation of the actual performance capabilities of wide bandgap semiconductors. To obtain a more accurate representation of the semiconductor materials'
performance characteristics, a thorough assessment of the trade-off curves from both Fig. 2.10 and Fig. 2.11 was carried out. It was found that only Fig. 2.10, which accounts for the dependencies of electric field and mobility on doping concentration and considers the incomplete ionization of donors and acceptors, captures a more realistic depiction of the wide bandgap semiconductors' true potential and performance capabilities.

2.9 Conflicting BV-$R_{on,sp}$ trade-offs in Diamond

Multiple research groups have investigated the impact ionization coefficients of diamond [16]-[19]. Due to variations in the maturity level of the diamond semiconductor material, a significant disparity exists among the reported impact ionization coefficients yielding a plethora of conflicting performance trade-off curves.

![Graph](image.png)

**Figure 2.12:** Critical field for avalanche breakdown in a diamond at 25°C evaluated from the impaction ionization coefficients reported by various research groups [16]-[19]
Fig. 2.12 illustrates the evaluated critical electric field's dependency on doping concentration at the breakdown for diamond at 25\(^\circ\)C, derived from impact ionization coefficients reported by Watanabe [16], Hiraiwa[17], Kamakura [18] and Rashid [19]. It is evident that there is a significant discrepancy in the critical electric fields, which arises from variations in the impact ionization coefficients of these groups.

![Graph showing critical electric field's dependency on doping concentration.](image)

**Figure 2.13:** Breakdown voltage dependence on the doping concentration in diamond; the plot also includes the overlay of experimental results reported in the literature

Moving to Fig. 2.13, we observe the breakdown voltage dependence on the doping concentration in the diamond. The plot also includes the overlay of experimental results reported in the literature. At this stage of research, the experimental data exhibit considerable variability, mirroring the disparities found in the impact ionization coefficients from different research groups. In Fig. 2.14, the trade-off relationship between specific on-resistance and breakdown voltage in diamond while considering the critical electric field and mobility dependencies on doping concentration, as well as the incomplete ionization of acceptors is explored. It is worth noting that
some impact ionization coefficients offer more favorable trade-off characteristics but however, the trade-off still lies between traditional silicon (Si) and 4H-SiC due to significantly low ionization of acceptors at 25°C (as shown in Fig. 2.4).

**Figure 2.14:** The trade-off relationship between specific on-resistance and breakdown voltage in diamond while considering the critical electric field and mobility dependencies on doping concentration, as well as the incomplete ionization of acceptors.

To summarize, the selection of appropriate impact ionization coefficients plays a pivotal role in conducting trade-off analyses accurately. The performance trade-offs are directly influenced by the choice of impact ionization coefficients, which, in turn, are contingent upon factors such as material quality, device design, and the effectiveness of edge termination techniques. Therefore, the author of this report acknowledges the criticality of meticulous scrutiny and cautious selection of impact ionization coefficients from the existing literature to ensure accurate assessment and optimization of trade-off performance parameters.
2.10 Efficient drift layer design for unipolar power devices in 4H-SiC

The prime objectives of this section [32] include i) to derive direct generalized expressions for \( N_D \), \( W_D \), and \( R_{on,sp} \) of NPT and PT structures, ii) comparing the impact of NPT and PT design structures on the drift parameters and correlating them.

In general, the critical electric field relation of Konstantinov [7], (13) is widely used to design the drift parameters in 4H-SiC due to its accuracy. In this section, a fitted version of Konstantinov’s critical electric field relation is used to derive the generalized optimum parameters for the drift design. The derived set of equations not only offers a straightforward design of optimum drift parameters avoiding complex mathematical evaluations but also provides a meaningful insight into the drift design in 4H-SiC. From derived expressions, an interrelation between the optimum punch-through and non-punch-through structures is attained. For the punch-through structure, it was observed that the optimum doping concentration and width for Konstantinov critical electric field model are 8% and 21.4% lower than that of the non-punch-through structure. Consequently, the specific on-resistance for the punch-through structure is 14.9% lower than that of the non-punch-through structure.

The critical electric field in 4H-SiC approximated by Konstantinov [7] is presented as

\[
E_c = \frac{2.49 \times 10^6}{1 - 0.25\log_{10}\left(\frac{N_D (cm^{-3})}{10^{16}}\right)} [V/cm] \quad (13)
\]

The \( E_c \) represented in (13) was evaluated based on an NPT structure which is plotted in Fig. 2.15. The critical electric field of NPT structures experiences an acute dependence on the
doping concentration, whereas in PT structures the critical electric field depends on both doping concentration and width of the drift layer. The analysis in [31], conveys that there is nearly no difference in the critical electric fields of PT and NPT structures at higher doping concentrations, but the distinction of critical electric fields gets more significant at comparatively lower doping concentrations for narrow widths of PT structures. For a reasonable doping range of $4 \times 10^{14}$ cm$^{-3}$ to $2 \times 10^{16}$ cm$^{-3}$ to accommodate most of the voltage ratings (600V-25kV) with reasonable widths of the drift layer, we confirmed that the difference in the critical electric fields for PT and NPT structures is negligible. Hence, it was assumed that the maximum critical electric fields at the breakdown in PT and NPT structures were equal in this study.

The breakdown voltage of a PT structure which is also the area of trapezoid $A_1$ in Fig. 2.2 is given by [1]

$$BV_{PT} = E_{c,PT} W_{PT} - \frac{qN_{D,PT} W_{PT}^2}{2\varepsilon_s} [V] \quad (14)$$

The computation and evaluation to optimize drift parameters using Konstantinov’s model from (13) is complex and time-consuming. For instance, when Konstantinov’s $E_c$ model from (13) is substituted into (14) results in (15) which is given by

$$\left(\frac{qN_{D,PT}}{2\varepsilon_s}\right) W_{PT}^2 - \left(\frac{2.49 \times 10^6}{1 - 0.25\log_{10}\left(\frac{N_{D,PT}}{10^{16}}\right)}\right) W_{PT} + BV_{PT} = 0 \quad (15)$$
The value of $W_{PT}$ is evaluated by solving the compounded quadratic expression (15). Not only that (15) is complex to solve, but for a specific value of $BV$, there are a wide range of solutions for $N_D$, $W_{PT}$, and $W_{PT}$ which makes it difficult to find a unique solution for the optimum specific on-resistance. On that account, to evaluate the solutions for the optimum design and to simplify the complications involved in (15), we performed a graphical curve fitting strategy to approximate the Konstantinov’s $E_c$ model as shown in Fig. 2.15. The approach of curve fitting reduces the complex $E_c$ relation from (13) to a simple form of $E_c = c_1 N_D^k$ with a minimum deviation from the original analytical model. The fitted model authorizes to provide of simple relations between $N_D$ and $BV$, $W_D$, and $BV$, and $R_{on}$ and $BV$. Hence, for a specific desired $BV$, the optimum $N_D$, $W_D$, and $R_{on}$ can be easily realized using the derived expressions. The curve fitting of the Konstantinov model is

**Figure 2.15:** Power series curve fitting of Konstantinov’s $E_c$ Model over doping range of $4 \times 10^{14}$ cm$^{-3}$ to $2 \times 10^{16}$ cm$^{-3}$ in 4H-4H-SiC; Solid line represents the analytical model and dotted line represents fitted model; Equation of the fitted model is provided in the inset ($E_c = 75750 N_D^{0.095}$).
performed in the doping range of $4 \times 10^{14}$ cm$^{-3}$ to $2 \times 10^{16}$ cm$^{-3}$. This doping latitude typically corresponds to the breakdown operational range of unipolar devices in 4H-SiC. The expression for $E_c$ of the fitted Konstantinov’s model is given by

$$E_c = 75750N_D^{0.095}[V/cm] \quad (16)$$

Here the units of $N_D$ is cm$^{-3}$. The coefficient 75750 and exponent 0.095 from (16) are denoted as $c_1$ and $k$, respectively to simplify and have a clear understanding of the further derivation of equations for generalized forms. So, the expression for $E_c$ of the fitted Konstantinov model is re-represented as

$$E_c = c_1N_D^k \quad (17)$$

For a PT structure, the specific on-resistance $R_{sp,PT}$ of a drift layer with a thickness of $W_{PT}$ is given by [1]

$$R_{sp,PT} = \frac{W_{PT}}{q\mu_nN_{D,PT}^+}[\Omega \cdot \text{cm}^2] \quad (18)$$

Here $\mu_n$ is the mobility parallel to c-axis and $N_{D,PT}^+$ is the at a doping of $1 \times 10^{17}$ cm$^{-3}$ and almost entirely ionized (98%) when the doping is below $3 \times 10^{16}$ cm$^{-3}$ [2], [32]. Since the doping latitude considered in this study is $4 \times 10^{14}$ cm$^{-3}$ to $2 \times 10^{16}$ cm$^{-3}$, it was assumed that donors are fully ionized ($N_{D,PT}^+ = N_{D,PT}$) at room temperature.

Hence by substituting $W_{PT}$ from (14) into (18), we obtain

$$R_{sp,PT} = \frac{c_1\varepsilon_sN_{D,PT}^{k-2}}{q^2\mu_n} \left[1 - \sqrt{1 - \frac{2qBV_{PT}N_{D,PT}^{1-2k}}{c_1^2\varepsilon_s}}\right] \quad (19)$$
Figure 2.16: The specific on-resistance of a 10kV drift layer designed using Konstantinov’s $E_c$ model in 4H-SiC; Optimum doping level to get the lowest specific on-resistance $(54.9\, \text{mΩ} \cdot \text{cm}^2)$ is $9.7 \times 10^{14} \, \text{cm}^{-3}$

To contemplate the approach to determine the optimum $R_{\text{sp,PT}}$ from (19), the drift design for a targeted BV of 10kV using Konstantinov’s $E_c$ model is considered. Substituting the value of targeted BV in (19), we have a wide range of values for $R_{\text{sp,PT}}$ for every value of $N_{D,PT}$ as shown in Fig. 2.16. The optimum design for drift layer is obtained for the lowest possible value of $R_{\text{sp,PT}}$ from Fig. 2.16 at a distinct doping concentration of $N_{D,PT}$. Through the conventional approach, performing graphical analysis on (19) to find the lowest possible $R_{\text{on,sp}}$ is often time-consuming and prone to a margin of error. So, to hold off from the implications and to find the minimum value of $R_{\text{sp,PT}}$ for the corresponding doping concentration ($N_{D,PT}$), the first derivative of (19) concerning $N_{D,PT}$ is performed and equated zero.

The repercussion of the derivative yields the optimum generalized parameters of a drift layer using PT design that apply to 4H-SiC whose critical electric field is in the form of $E_c = c_1 N_D^k$. 
The generalized forms of drift layer parameters of PT design in 4H-SiC are summed up in Table 2.2. It should be noted that BV\textsubscript{PT} or BV\textsubscript{NPT} in the generalized expressions of Table 2.2 and Table 2.3 is represented as BV as it is a desired entity and it remains the same for either PT or NPT design.

To find the minimum value of \( R_{sp,PT} \), the first derivative of (19) concerning \( N_{D,PT} \) is performed and equated to zero.

\[
\frac{dR_{sp,PT}}{dN_{D,PT}} = 0 \quad (20)
\]

\[
\left[ \sqrt{1 - \frac{2qBV_{PT}N_{D,PT}^{1-2k}}{c_1^2\varepsilon_s}} \right] \times \left[ 1 - \sqrt{1 - \frac{2qBV_{PT}N_{D,PT}^{1-2k}}{c_1^2\varepsilon_s}} \right] = -\left( \frac{1 - 2k}{k - 2} \right) \times \frac{qBV_{PT}N_{D,PT}^{1-2k}}{c_1^2\varepsilon_s} \quad (21)
\]

To solve (21), let

\[
\sqrt{1 - \frac{2qBV_{PT}N_{D,PT}^{1-2k}}{c_1^2\varepsilon_s}} = x \quad (22)
\]

Substituting (22) into (21), and solving for \( x \),

\[
x = \frac{1}{3} (1 - 2k) \quad (23)
\]

Substituting (23) into (22)

\[
\sqrt{1 - \frac{2qBV_{PT}N_{D,PT}^{1-2k}}{c_1^2\varepsilon_s}} = \frac{1}{3} (1 - 2k) \quad (24)
\]

Solving (24) for the generalized form of the optimum doping concentration of PT structure \( N_{D,PT} \) is given as
\[ N_{D,PT} = \left[ \frac{4}{9} (-k^2 + k + 2) \left( \frac{c_1^2 \varepsilon_s}{2qBV} \right) \right]^{\frac{1}{1-2k}} \] (25)

Substituting (25) into (19), the generalized form for the optimum width of PT structure \(W_{PT}\) is given by

\[ W_{PT} = \frac{2 c_1 \varepsilon_s}{3 q} (1 + k) \left[ \frac{4}{9} (-k^2 + k + 2) \left( \frac{c_1^2 \varepsilon_s}{2qBV} \right) \right]^{\frac{k-1}{1-2k}} \] (26)

Substituting (25) and (26) into (19), the generalized form of optimum specific on-resistance of PT structure \(R_{sp,PT}\) is given by

\[ R_{sp,PT} = \frac{2 c_1 \varepsilon_s}{3 q^2 \mu_n} (1 + k) \left[ \frac{4}{9} (-k^2 + k + 2) \left( \frac{c_1^2 \varepsilon_s}{2qBV} \right) \right]^{\frac{k-2}{1-2k}} \] (27)

**Table 2.2:** Derived generalized forms of drift layer parameters for PT design applicable to 4H-SiC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Generalized forms of PT Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>(N_{D,PT})</td>
<td>[ \left[ \frac{4}{9} (-k^2 + k + 2) \left( \frac{c_1^2 \varepsilon_s}{2qBV} \right) \right]^{\frac{1}{1-2k}} ]</td>
</tr>
<tr>
<td>(W_{PT})</td>
<td>[ \frac{2 c_1 \varepsilon_s}{3 q} (1 + k) \left[ \frac{4}{9} (-k^2 + k + 2) \left( \frac{c_1^2 \varepsilon_s}{2qBV} \right) \right]^{\frac{k-1}{1-2k}} ]</td>
</tr>
<tr>
<td>(R_{sp,PT})</td>
<td>[ \frac{2 c_1 \varepsilon_s}{3 q^2 \mu_n} (1 + k) \left[ \frac{4}{9} (-k^2 + k + 2) \left( \frac{c_1^2 \varepsilon_s}{2qBV} \right) \right]^{\frac{k-2}{1-2k}} ]</td>
</tr>
</tbody>
</table>

By substituting \(c_1\), \(k\), and the values of \(q\), \(\varepsilon_s\) and \(\mu_n\) of 4H-SiC in Table 2.2, the optimum drift layer parameters of PT structure to achieve a specified BV in 4H-SiC is encapsulated and summarized in Table 2.4.
**NPT design**

The drift parameters of NPT design using the Konstantinov $E_c$ relation are derived in this subsection. From Fig. 2.1, the maximum value of $E(x)$ at $x=0$, gives the critical electric field $E_c$, given by

$$E_{c,NPT} = \frac{qN_{D,NPT}W_{NPT}}{\varepsilon_s} [V/cm] \quad (28)$$

The breakdown of NPT structure and also the area of the triangle $A_2$ from Fig. 2.1 is given by

$$BV_{NPT} = \frac{1}{2}E_{c,NPT}W_{NPT}[V] \quad (29)$$

The doping concentration of the NPT structure for a desired breakdown voltage is given by

$$N_{D,NPT} = \frac{\varepsilon_sE_{c,NPT}^2}{2qBV_{NPT}} [cm^{-3}] \quad (30)$$

The critical electric field $E_c$, for a NPT structure is given by

$$E_{c,NPT} = \frac{qN_{D,NPT}W_{NPT}}{\varepsilon_s} [V/cm] \quad (31)$$

Trading (16) into (29), for the generalized form of the doping concentration of NPT structure ($N_{D,NPT}$) is given as

$$N_{D,NPT} = \left( \frac{c_1^2\varepsilon_s}{2qBV} \right)^{\frac{1}{1-2k}} \quad (32)$$

From (29) and (30),

$$W_{NPT} = \frac{\varepsilon_sE_{c,PP}}{qN_{D,NPT}} [cm] \quad (33)$$

Substituting (16) and (31) into (32), the generalized form for the width of NPT structure ($W_{NPT}$)
is given by

\[ W_{\text{NPT}} = \left[ \left( \frac{q}{\varepsilon_s} \right)^k \frac{1}{c_1(2BV)^{k-1}} \right]^{1-2k} \] (34)

Similar to (20), the specific on-resistance of NPT (R_{\text{sp,NPT}}) design is given by

\[ R_{\text{sp,NPT}} = \frac{W_{\text{NPT}}}{q\mu_n N_{\text{NPT}}^+} \] (35)

Substituting (31) and (33) into (34), the generalized form for the specific on-resistance of NPT (R_{\text{sp,NPT}}) design is given by

\[ R_{\text{sp,NPT}} = \frac{1}{\mu_n} \left[ \left( \frac{q}{c_1} \right)^3 \frac{1}{\varepsilon_s^{1+k}} \left( \frac{1}{(2BV)^{k-2}} \right) \right]^{1-2k} \] (36)

**Table 2.3:** Derived generalized forms of drift layer parameters for NPT design applicable to 4H-SiC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Generalized forms of NPT Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>N_{D,NPT}</td>
<td>( \left( \frac{c_1^2 \varepsilon_s}{2qBV} \right)^{1-2k} )</td>
</tr>
<tr>
<td>W_{NPT}</td>
<td>[ \left( \frac{q}{\varepsilon_s} \right)^k \frac{1}{c_1(2BV)^{k-1}} ]^{1-2k}</td>
</tr>
<tr>
<td>R_{sp,NPT}</td>
<td>[ \frac{1}{\mu_n} \left[ \left( \frac{q}{c_1} \right)^3 \frac{1}{\varepsilon_s^{1+k}} \left( \frac{1}{(2BV)^{k-2}} \right) \right]^{1-2k} ]</td>
</tr>
</tbody>
</table>

Table 2.3 summarizes all the derived generalized forms for the doping concentration, width, and specific on-resistance of NPT structure. Hence, if the electric field dependence on the doping concentration of a semiconductor and targeted BV is known, the optimum parameters for
the drift layer can be obtained by directly substituting the coefficient and exponent of doping concentration.

By substituting $c_1$, $k$, and the values of $q$, $\varepsilon$, and $\mu_n$ of 4H-SiC in Table 2.3, the optimum drift layer parameters of NPT structure to achieve a specified BV in 4H-SiC is encapsulated and summarized in Table 2.4.

**Table 2.4:** Summary of derived drift parameters for PT and NPT structures for 4H-SiC power using Konstantinov’s model

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Konstantinov’s fitted $E_c$ model. $E_c = 75750 N_D^{0.095}$ [V/cm]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PT (Derived in this work)</td>
</tr>
<tr>
<td>$N_D$ (cm$^{-3}$)</td>
<td>$8.839 \times 10^{19}BV^{-1.234}$</td>
</tr>
<tr>
<td>$W_D$ (cm)</td>
<td>$2.625 \times 10^{-7}BV^{1.117}$</td>
</tr>
<tr>
<td>$R_{on,sp}(\Omega cm^2)$</td>
<td>$2.791 \times 10^{-11}BV^{2.296}$</td>
</tr>
<tr>
<td></td>
<td>$2.95 \times 10^{-11}BV^{2.28}$ [32]</td>
</tr>
<tr>
<td></td>
<td>NPT (Derived in this work)</td>
</tr>
<tr>
<td></td>
<td>$9.602 \times 10^{19}BV^{-1.234}$</td>
</tr>
<tr>
<td></td>
<td>$3.336 \times 10^{-7}BV^{1.117}$</td>
</tr>
<tr>
<td></td>
<td>$3.278 \times 10^{-11}BV^{2.296}$</td>
</tr>
</tbody>
</table>

Derived generalized forms of drift layer parameters for NPT design applicable to 4H-SiC summarized in Table 2.4 along with optimum drift parameters of PT structure. Hence the optimum doping concentration, width, and specific on-resistance of the drift layer can be determined directly by substituting the value of BV in the summarized equations of Table 2.4.

The above go-to expressions from Table 2.4 discloses that the optimum doping concentration, width, and specific on-resistance of the drift layer can be determined directly by substituting the value of BV avoiding the complex mathematical evaluations. An updated trade-off limit between specific on-resistance and breakdown voltage reported in [32] is also included in Table 2.4 and plotted in Fig. 2.18.
Comparative analysis

Contemplating the equations of doping concentration, width, and specific on-resistance of PT and NPT designs from Table 2.4, it is evident that the drift design parameters of PT and NPT structures in Konstantinov $E_c$ relation are co-related by a constant value. Fractionating the corresponding parameters of PT and NPT from Table 2.4, we have

$$N_{PT,K} = 0.920 N_{NPT,K}$$ \hspace{1cm} (37)

Dividing optimum values of widths of PT and NPT,

$$W_{PT,K} = 0.786 W_{NPT,K}$$ \hspace{1cm} (38)

The ratio of on-resistances of PT and NPT from Table 2.4 yields,

**Figure 2.17:** Doping concentration and width dependence on breakdown voltage (600V to 25kV) of NPT and PT structures in 4H-SiC; Doping concentration of PT (plain line) structure is 8% less than NPT (dotted line) and width of PT is 21.4% less than NPT.
$R_{PT,K} = 0.851 R_{NPT,K}$ (39)

It is concluded that from (37, 38, and 39), at a distinct BV, the doping concentration and width of the drift layer of a PT structure need to be reduced approximately by 8% and 21.4% respectively, when compared to the NPT structure. Fig. 2.17 plots the required doping concentrations and widths of drift layers for PT and NPT structures using Konstantinov’s $E_c$ model to achieve a specific BV. Hence, Fig. 2.17 provides a graphical design guideline for drift layer design in 4H-SiC based power devices.

The trade-off relation between specific on-resistance and breakdown voltage is plotted in Fig. 2.18. As anticipated, at a specific breakdown voltage, the PT structure offers 14.9% lower specific on-resistance when compared to the NPT structure. The 4H-SiC limit of the PT structure

![Figure 2.18](image)

**Figure 2.18:** Trade-off relation between specific on-resistance and breakdown voltage (600V to 25kV) of NPT and PT structures in 4H-SiC; Specific on-resistance of PT is 14.9% of that of NPT in 4H-SiC [33]; Updated specific on-resistance of PT structure from [32] is also indicated
from this study using Konstantinov’s $E_c$ model agrees with [32] at lower breakdown voltages but there is a minute increase in $R_{on,sp}$ at higher breakdown voltages when compared to [32] as indicated in Fig. 2.18. This disparity in the $R_{on,sp}$ is partly attributed to the different critical electric field models used.

**2.11 NPT versus PT – dynamic performance**

In this section, the focus is on discussing the dynamic performance comparison of NPT and PT designs. As demonstrated in the preceding sections, it is evident that the PT design offers a lower specific on-resistance in comparison to the NPT design. This reduction in resistance in the PT design brings clear advantages, such as lower conduction losses or the possibility of using smaller dies while achieving the same specific on-resistance. Moreover, the smaller chip size in PT designs can lead to lower capacitances, gate charges, and output charges, resulting in reduced dynamic losses during switching events. These benefits contribute to improved switching characteristics and overall device performance.

However, it is essential to consider the potential drawbacks of PT designs as well. The reduced chip size in PT devices may have an adverse impact on their current and power ratings. Larger die sizes, characteristic of NPT designs, allow for lower current density and better heat sink capabilities, which enhance the ruggedness of the devices. Consequently, for a given on-resistance, NPT designs are inherently more rugged compared to PT designs. When evaluating the benefits of PT designs based on their specific on-resistance advantage, it is crucial to also take into account the potential disadvantages related to ruggedness.

In summary, the dynamic performance of PT designs showcases advantages in terms of lower specific on-resistance and reduced dynamic losses during switching. However, one must be
mindful of the ruggedness disadvantage stemming from the smaller chip size. A careful evaluation of both aspects is necessary to make informed decisions in the design and selection of drift layer for power semiconductor devices.

2.12 Conclusions

In conclusion, this chapter offers an in-depth exploration of drift layer design in wide bandgap semiconductors, specifically focusing on 4H-SiC. The comprehensive trade-off analysis conducted in this chapter encompasses critical factors such as breakdown voltage assessment, impact ionization coefficients, critical electric field dependence on doping concentration, and the importance of incomplete ionization for specific on-resistance considerations. The insights gained from this analysis empower researchers to make informed decisions when optimizing the non-punch-through (NPT) drift layer design for wide bandgap semiconductors. Furthermore, the chapter delves into the drift layer design for unipolar power devices within the voltage range of 600V to 25kV, with particular emphasis on 4H-SiC. Both NPT and punch-through (PT) designs are explored, and simplified generalized equations are derived using mathematical power series curve fitting techniques. These equations serve as invaluable design guidelines, offering profound insights into selecting appropriate drift layer architectures based on the desired voltage rating.

2.13 References


CHAPTER 3: SMART IC Process Overview

3.1 Introduction

Based on the team’s experience fabricating SMART 4H-SiC Power ICs at the Analog Devices, Inc. (ADI) Hillview fabrication facility, and its continued experience fabricating SMART 4H-SiC Power ICs at the SiCamore Semi fabrication facility located in Bend, OR, a sufficient understanding of the necessary manufacturing capabilities were acquired to unravel this technology. This chapter intends potential entry for any IC chip company to complete a full manufacturing run of a SMART 4H-SiC Power IC technology. The key aspects that ought to be considered when it comes to starting materials, fabrication process flow, device designs, and high-voltage and low-voltage integration are highlighted. The content in this chapter also equips the designers with significant simulated/experimental information on the fabricated components to authorize design success. Up to this point, two lots were fabricated at ADI fab with its feature size of 0.5 μm and two other lots are currently being fabricated at the SiCamore fabrication facility where the feature size is 1 μm. Working with different fabs with two different toolsets and 4H-SiC wafer processing capabilities (4 in. vs 6 in.), the boundaries of critical process parameters are better understood and defined, especially when previous lot measurement data is considered. Overall, this process control document acts as a guideline for achieving stable and compatible technology by creating a robust supply chain (substrate, epi stack) and incorporation of specialty processes (gate oxide, ILD, contacts), tuned specifically for N-type vs P-type and Power vs CMOS devices for timely development, processing, and delivery to the end customers. The process flow, device, and circuit designs of Lot 2, which significantly and completely capture the implementation of SMART IC technology were used in shaping this chapter.
3.2 Component List

The significant component list that was fabricated in SMART IC technology is summarized in Table 3.1.

**Table 3.1:** List of components fabricated with SMART IC technology.

<table>
<thead>
<tr>
<th>List of Components</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>400-600 V Lateral Power n-type MOSFET (HV NMOS)</td>
<td></td>
</tr>
<tr>
<td>30-40V n-type MOSFET (LV NMOS)</td>
<td></td>
</tr>
<tr>
<td>30-40V p-type MOSFET (LV PMOS)</td>
<td></td>
</tr>
<tr>
<td>Transmission Line Measurement patterns (TLM) (n-type and p-type)</td>
<td></td>
</tr>
<tr>
<td>FAT FETs (n-type and p-type)</td>
<td></td>
</tr>
<tr>
<td>Poly to Well capacitors</td>
<td></td>
</tr>
<tr>
<td>Metal-Metal capacitors</td>
<td></td>
</tr>
<tr>
<td>Diffusion capacitors</td>
<td></td>
</tr>
<tr>
<td>N+ resistors</td>
<td></td>
</tr>
<tr>
<td>P+ resistors</td>
<td></td>
</tr>
<tr>
<td>Gate poly resistors</td>
<td></td>
</tr>
<tr>
<td>Metal resistors</td>
<td></td>
</tr>
</tbody>
</table>

3.3 Layers and Component to Layer matrix

Table 3.2 shows the layers, GDS, and corresponding drawn specifications of the SMART IC technology. The component-to-layer matrix is shown in Table 3.3.
Table 3.2: Layer, GDS, and drawn specification of SMART IC technology

<table>
<thead>
<tr>
<th>Process</th>
<th>GDS layer</th>
<th>Drawn is</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero</td>
<td>1</td>
<td>Etched</td>
</tr>
<tr>
<td>P Well</td>
<td>2</td>
<td>Implanted</td>
</tr>
<tr>
<td>P top</td>
<td>3</td>
<td>Implanted</td>
</tr>
<tr>
<td>P-Iso</td>
<td>4</td>
<td>Implanted</td>
</tr>
<tr>
<td>N Well</td>
<td>5</td>
<td>Implanted</td>
</tr>
<tr>
<td>N+</td>
<td>6</td>
<td>Implanted</td>
</tr>
<tr>
<td>P+</td>
<td>7</td>
<td>Implanted</td>
</tr>
<tr>
<td>Gate Poly</td>
<td>8</td>
<td>Gate</td>
</tr>
<tr>
<td>Ohmic contact</td>
<td>9</td>
<td>Ohmic</td>
</tr>
<tr>
<td>Poly Contact</td>
<td>10</td>
<td>Etched</td>
</tr>
<tr>
<td>Metal 1</td>
<td>11</td>
<td>Metal</td>
</tr>
<tr>
<td>Via 1</td>
<td>12</td>
<td>Etched</td>
</tr>
<tr>
<td>Metal 2</td>
<td>13</td>
<td>Metal</td>
</tr>
<tr>
<td>Via 2</td>
<td>14</td>
<td>Etched</td>
</tr>
<tr>
<td>Metal 3</td>
<td>15</td>
<td>Metal</td>
</tr>
<tr>
<td>Pad</td>
<td>16</td>
<td>Etched</td>
</tr>
</tbody>
</table>
Table 3.3: Component-to-layer matching in SMART IC technology

<table>
<thead>
<tr>
<th>Component</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>P Well</td>
</tr>
<tr>
<td>HV NMOS</td>
<td>x</td>
</tr>
<tr>
<td>LV NMOS</td>
<td>x</td>
</tr>
<tr>
<td>LV PMOS</td>
<td>x</td>
</tr>
<tr>
<td>TLM</td>
<td>x</td>
</tr>
<tr>
<td>FAT FETs</td>
<td>x</td>
</tr>
<tr>
<td>Poly to Well cap</td>
<td>x</td>
</tr>
<tr>
<td>Diffusion cap</td>
<td>x</td>
</tr>
<tr>
<td>Metal-Metal cap</td>
<td>x</td>
</tr>
<tr>
<td>N+ resistors</td>
<td>x</td>
</tr>
<tr>
<td>P+ resistors</td>
<td>x</td>
</tr>
<tr>
<td>Poly resistors</td>
<td>x</td>
</tr>
<tr>
<td>Metal resistors</td>
<td>x</td>
</tr>
</tbody>
</table>
3.4 Process flow cross-sectional diagrams

HV Lateral MOSFET, LV NMOS, and LV PMOS are considered to demonstrate the detailed process flow for SMART IC technology. There are 16 masks and 6 implantation steps in this process flow.

Starting material (Epi layers on N+ Substrate)

The raw material utilized is a 6-inch double-side polished N+ substrate. It consists of a P-epi layer with a thickness of 6µm and a doping concentration of $2 \times 10^{16} \text{ cm}^{-3}$. Additionally, there is an N-drift layer with a thickness of 2.5µm and a doping concentration of $6.5 \times 10^{16} \text{ cm}^{-3}$.

Zero etch

To create an alignment mark crucial for process monitoring and control, the substrate undergoes a patterning step using mask 1 (M1) followed by etching and cleaning procedures.
**P Well PHOTO & Implant**

To establish the P Well region, Aluminum series implants are performed at room temperature, employing mask 2 (M2). For the ion implantation process, an oxide blocking layer is patterned, etched, and cleaned.

**P top PHOTO & Implant**

Similarly, the P top region is formed using Aluminum series implants at room temperature with the assistance of mask 3 (M3). An oxide blocking layer is patterned, etched, and cleaned again.

**P+ Isolation PHOTO & Implant**

For the implementation of the P-Iso (Isolation) region with a depth of 2.5µm, channeling implantation is employed.
N Well PHOTO & Implant

To form the N Well regions, Nitrogen series implants are performed at room temperature, utilizing mask 5 (M5). An oxide-blocking layer is patterned, etched, and cleaned in preparation for the ion implantation process.

N+ PHOTO & Implant

To create the N+ source and drain regions, Nitrogen series implants are carried out at approximately 600°C, employing mask 6 (M6).
P+ PHOTO & Implant

Similarly, for the P+ source and drain regions, Aluminum series implants are conducted at approximately 600°C, utilizing mask 7 (M7). An oxide blocking layer is patterned, etched, and cleaned for each of these ion implantation processes.

Gate Oxide formation

Implantation steps were followed by 1650°C and 10-min activation annealing with a carbon cap. The best gate oxide recipe as well as other candidate processes were used for gate oxide formation.

Gate Poly PHOTO, Deposition & Etch

Followed by gate oxide formation, a 500nm gate polysilicon is deposited, patterned using mask 8 (M8) and subsequently to polysilicon etch.
ILD 1 Deposition, CMP & Etch

An interlayer dielectric (ILD-1) was deposited. CMP was performed to planarize the surface. ILD-1 was etched using mask 9 (M9) to open the ohmic contact regions.

Simultaneous Ohmic Contact for both n-type and p-type

Nickel (Ni) was deposited on the front side, followed by low temperature annealing for the formation of Nickel silicide region. The un-silicided region on oxide was removed by wet etching.
After the ohmic contact formation on the front-side, mask 10 (M10) was used to etch the pads for the gate.

**Metal 1 Deposition, Pattern & Etch**

W plug was deposited followed by CMP process before the metal-1 deposition. As metal layer 1 (Metal-1), a 0.5 µm thick Al-based metal was deposited, patterned using mask 11 (M11) for the source, drain and the gate metal regions.

**ILD 2 Deposition, CMP & Etch**

An interlayer dielectric (ILD-2) was deposited. ILD-2 is patterned using mask 12 (M12) and etched.
**Metal 2 Deposition, Pattern & Etch**

Second metal layer (Metal-2) with similar thickness as Metal-1 (0.5 µm) was formed using mask 13 (M13).

**ILD 3 Deposition, CMP & Etch**

An interlayer dielectric (ILD-3) was deposited. ILD-3 was patterned using mask 14 (M14) and etched.

**Metal 3 Deposition, Pattern & Etch**

A third metal layer (Metal-3) with a thickness of >4 µm was deposited and patterned using mask 15 (M15).
Passivation/ Pad open

The final mask (M16) is used to passivate the front side with nitride and polyimide.
3.5 Process Design methodology

This section focuses on discussing the design approaches for both the front-end-of-line (FEOL) and back-end-of-line (BEOL) processes. It delves into the implant schedules, ohmic processes, and gate oxide processes that have been specifically designed and implemented for the SMART IC technology. Furthermore, the corresponding experimental data and simulation results associated with these processes are thoroughly explored and presented.

3.5.1 Starting material design

The initial phase commences with the careful selection of the epi stack or starting material, marking an important initial step. One of the notable distinguishing features of the SMART IC technology is the seamless integration of HV lateral MOSFET and LV CMOS components. Consequently, the specifications for the epi stack are designed with these specific requirements in mind.

The first objective is to attain a high voltage blocking capability for the HV lateral MOSFET. The second objective is to effectively isolate the high voltage blocks from the low voltage blocks within the integrated circuit. Therefore, the epi stack is configured to include a top layer of n-epi material to facilitate the design of HV Lateral MOSFET, while the bottom layer consists of p-epi material to ensure proper isolation. This careful selection and configuration of the epi stack align with the unique specifications (Fig. 3.1) of the SMART IC technology, enabling its successful implementation.
Figure 3.1: Starting material for the SMART IC technology with epi specifications

The simulations of the HV Lateral MOSFET design that were performed to determine the epi specifications are reported here. Fig. 3.2 shows the cross-sectional view with critical dimensions labeled for the proposed structure for HV Lateral MOSFET. This structure adopts a double REduced SURface Field (RESURF) concept utilizing the P-top and P-epi from the bottom to achieve the highest possible breakdown voltage in the lateral direction. A P-top layer (lightly doped) is adopted to reduce the surface electric field (RESURF) which helps in enhancing the breakdown voltage.

Figure 3.2: Schematic cross-section of the HV Lateral MOSFET
In order to optimize the doping concentration of the N-epi material, a thorough investigation of the trade-off relationship between BV and $R_{on,sp}$ was conducted through 2-D device simulations, as depicted in Fig. 3.3. The objective was to identify the doping concentration that would enable the device to withstand high voltages while minimizing the specific on-resistance. Fig. 3.3 clearly illustrates that a wide range of doping concentrations, ranging from $5.5 \times 10^{16} \text{ cm}^{-3}$ to $8.2 \times 10^{16} \text{ cm}^{-3}$, can achieve the target breakdown voltage of 700V. Correspondingly, the $R_{on,sp}$ varies between 5.3 mohm-$\text{cm}^2$ and 4.8 mohm-$\text{cm}^2$ within this range. After careful analysis, it was determined that the optimal doping concentration for the N-epi material is $6.5 \times 10^{16} \text{ cm}^{-3}$, as it strikes a balance between supporting a high voltage and minimizing the specific on-resistance.

![Figure 3.3: Simulation results for the trade-off relation between BV and Ron for various doping concentrations in the N-epi layer](image)

The P-epi layer serves a dual purpose as a double RESURF (Reduced Surface Field) to significantly enhance the breakdown voltage of the device. The doping concentration and thickness of the P-epi layer are meticulously optimized to support the highest achievable breakdown voltage
while effectively preventing the depletion layer from extending into the N+ Substrate. The occurrence of depletion layer reach-through, where it extends to the N+ Substrate, results in undesirable shorting of all devices and circuitry within the system. It is important to note that deviating from the optimal values of lower doping concentration and reduced thickness of the P-epi layer leads to the manifestation of reach-through phenomena. Fig. 3.4 illustrates the variation in breakdown voltage as the doping concentration in the P-epi layer is altered while maintaining a constant thickness of 6µm. At doping concentrations lower than $8 \times 10^{15}$ cm$^{-3}$, the P-epi completely depleted reach-through the N+ substrate which is undesirable for reliable power IC operation where two HV lateral MOSFETs are integrated on a single chip. Therefore, to attain the target breakdown voltage of 700V, the optimal values for the P-epi layer are determined to be a doping concentration of $2 \times 10^{16}$ cm$^{-3}$ and a thickness of 6µm. It is noteworthy that the variation in P-epi doping has a negligible impact on the $R_{on,sp}$ of the HV NMOS component, as expected.

![Graph showing the variation in breakdown voltage and specific on-resistance with varying P-epi doping concentration.](image)

**Figure 3.4:** Simulation results for the trade-off relation between BV and Ron for various doping concentration of P-epi
3.5.2 P Well layer

**Implant profiles and Critical dimensions:**

The implant schedules are designed using SRIM. To ensure the accuracy and effectiveness of the implant schedules, verification is carried out using Synopsis sProcess. The specific design and implant profiles of the P Well, an essential component of the integrated circuit, are extensively discussed and elaborated upon in section 7.2.1 of this thesis, providing comprehensive insights into their characteristics and implementation. The critical dimensions of the P Well process is shown in Table 3.4.

**Table 3.4:** Critical dimensions (CD) for the P Well process

<table>
<thead>
<tr>
<th>Target Critical Dimensions for P Well</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>------------</td>
</tr>
<tr>
<td>Line</td>
</tr>
<tr>
<td>Space</td>
</tr>
</tbody>
</table>

**Note:** Line is the dimension of oxide/PR after patterning & Space is the dimension between oxide/PR after patterning

3.5.3 P top

**Implant profiles and Critical dimensions:**

Aluminum is used as an implant element to form the p-type layer. The implant profile of P top is shown in Fig. 3.5. The dose of the P top was designed to prevent complete depletion that results in increased electric field in the oxide and reduction in the breakdown voltage as shown in section 4.2.1 of this thesis. The critical dimensions of the P top process are shown in Table 3.5.
Figure 3.5: Implant profile of the P top

Table 3.5: Critical dimensions (CD) for the P top process

<table>
<thead>
<tr>
<th>Target Critical Dimensions for P top</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>Dimensions (μm)</td>
</tr>
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<td>0.8</td>
</tr>
<tr>
<td>Space</td>
<td>4.5</td>
</tr>
</tbody>
</table>

Note: **Line** is the dimension of oxide/PR after patterning & **Space** is the dimension between oxide/PR after patterning

### 3.5.4 P+ Isolation

_Specifications and Critical dimensions:

In the pursuit of advancing single-chip HV (High-Voltage) Power ICs solutions, the isolation of Low-Voltage (LV) entities from High-Voltage devices becomes an indispensable requirement. In this study, the adoption of junction isolation plays a pivotal role in safeguarding_
the LV blocks from the influence of high voltages. To achieve effective isolation, a combination of P+ Isolation and P-epi layers is employed to create a barrier between the potentials of the N-epi and adjacent components.

The implementation of P+ junction isolation is carried out through channeling implantation, wherein ions are implanted at a 0-degree angle normal to the crystallographic orientation [0001]. This technique aids in the creation of well-defined isolation regions. The design, efficacy, and optimization strategies employed for this junction isolation method are extensively discussed in section 5.3 of this thesis, providing a comprehensive analysis of its characteristics and performance. The critical dimensions of the P+ Isolation process are shown in Table 3.6.

Table 3.6: Critical dimensions (CD) for the P+ Isolation process

<table>
<thead>
<tr>
<th>Target Critical Dimensions for P+ Isolation</th>
<th>Parameter</th>
<th>Dimensions (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Line</td>
<td>5.4</td>
</tr>
<tr>
<td></td>
<td>Space</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Note: Line is the dimension of oxide/PR after patterning & Space is the dimension between oxide/PR after patterning

3.5.5 N Well

Implant profiles and Critical dimensions:

The formation of N Wells in the SMART IC technology involves the utilization of Nitrogen implants. Section 7.2.2 of this document focuses on the in-depth exploration of well design
techniques, specifically addressing the accumulation mode and inversion mode with experimental validation as part of the comprehensive investigation outlined in this section. The critical dimensions of the N Well process is shown in Table 3.7.

**Table 3.7: Critical dimensions (CD) for the N Well process**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Dimensions (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line</td>
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</tr>
<tr>
<td>Space</td>
<td>32</td>
</tr>
</tbody>
</table>

*Note: Line is the dimension of oxide/PR after patterning & Space is the dimension between oxide/PR after patterning*

### 3.5.6 N+

**Implant profiles and Critical dimensions:**

A highly doped nitrogen implant is used to establish the N+ region within the devices, specifically for the source, drain, or body regions. The implant profile of the N+ region, graphically depicting the distribution and concentration of implanted nitrogen ions, is presented in Fig. 3.6. The critical dimensions of the N+ process is shown in Table 3.8.
3.5.7 P+

*Implant profiles and Critical dimensions:*

To establish the P+ region in the devices, a highly doped Aluminum implantation process is employed for the source, drain, and body regions. The implantation profile of the P+ region,
capturing the spatial distribution and concentration of the implanted Aluminum ions, is explicitly depicted in section 7.4 of this document. This section delves into comprehensive research and analysis of the impact of the P+ doping profile on the contact resistance, providing valuable insights into the relationship between doping characteristics and electrical performance. The investigation sheds light on the optimization of the P+ implantation process to mitigate contact resistance and enhance overall device functionality. The critical dimensions of the P+ process are shown in Table 3.9.

### Table 3.9: Critical dimensions (CD) for the P+ process

<table>
<thead>
<tr>
<th>Target Critical Dimensions for N+</th>
<th>Dimensions (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td></td>
</tr>
<tr>
<td>Line</td>
<td>1</td>
</tr>
<tr>
<td>Space</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Note: **Line** is the dimension of oxide/PR after patterning & **Space** is the dimension between oxide/PR after patterning.

#### 3.5.8 Gate oxide

Multiple gate oxide recipes, encompassing diverse combinations of post oxidation annealing timings, the use of thermal oxide versus deposited oxides, and variations in oxide thicknesses, were implemented to achieve optimal channel mobilities and superior dielectric properties. In-depth analysis and discussion of the split conditions and their corresponding electrical characteristics, including field effect mobilities and threshold voltage (Vth), are thoroughly explored in section 7.3 of this document.
3.5.9 Ohmic process

For the SMART IC technology, a single ohmic metal (Ni) process was employed to achieve the simultaneous formation of both n-type and p-type ohmic contacts on 4H-SiC. However, dedicated efforts have been made to enhance the contact resistance specifically for the p-type contacts. Section 7.4 of this document provides an extensive discussion on two research aspects undertaken to address this issue.

A comprehensive analysis of the detailed ohmic process is presented, incorporating information regarding the metal thicknesses employed, conditions for Rapid Thermal Annealing (RTA), and corresponding Transmission Line Measurement (TLM) results. These findings shed light on the intricacies of the ohmic process, serving as a valuable resource for understanding the interplay between process parameters, metal thickness, annealing conditions, and resulting contact resistances in the context of the SMART IC technology.

3.5.10 Multi-metal layered BEOL process

The implementation of a multi-layered metal scheme is an essential and advantageous feature in the pursuit of robust, scalable, and reliable High-Voltage (HV) power ICs. In the context of the SMART IC technology, a three-metal layered process is integrated to facilitate flexible metal routings and the establishment of resilient designs. However, ensuring the Insulator Layer Dielectric (ILD) between the metal layers can withstand high voltages is critical to guarantee reliable operation.

Section 5.4 of this document presents a comprehensive account of the investigation into the SEM cross-section and ILD breakdown characteristics, which were precisely measured from
Metal-Insulator-Metal (MIM) capacitors. These measurements provide valuable insights into the structural integrity of the ILD and its ability to withstand high voltages.
4.1 Introduction

In contrast to the prevailing vertical architecture, the proposed 4H-SiC power IC technology necessitates the utilization of a lateral architecture for the high-voltage (HV) power switch. This chapter focuses on the design and experimental demonstration of HV lateral MOSFETs and diodes in 4H-SiC, specifically tailored for integration within power ICs. The comprehensive development process encompasses simulations and in-depth analysis of experimental results pertaining to these devices are reported in this chapter. Followed by the designs and characterizations, a trade-off comparison has been included contemplating the devices reported in this work to that of the ones reported in the literature [1]-[16]. The initial phase of HV device development was experimentation on an N-epi/N+ substrate (Fig. 4.1), followed by successful implementation on the N-epi/P-epi/N+ substrate (Fig. 4.2), which is the compatible substrate option for power IC fabrication.

**Figure 4.1:** Cross-section showing the monolithic integration of the HV lateral MOSFET, LV NMOS, and LV PMOS on an N-epi grown on an N+ substrate
Figure 4.2: Cross-section showing the monolithic integration of the HV lateral MOSFET, LV NMOS, and LV PMOS on an N-epi, P-epi grown on N+ substrate

4.2 HV lateral devices on N-epi/N+ substrate

A 6 µm, $2.4 \times 10^{16}$ cm$^3$ doped N-type epi-layer on an N+ substrate was used for the fabrication of the reported HV lateral MOSFETs and diodes. Nitrogen (N) and Aluminum (Al) implants are used to form the N+source/drain regions and P Well, P top, and P+ source regions respectively. A single process flow is used to fabricate all the devices.

4.2.1 Nominal HV lateral MOSFET design

Fig. 4.3 presents the schematic cross-section of the fabricated HV lateral MOSFET on the N-epi/N+ substrate. The depicted schematic provides a detailed representation of the structural composition and arrangement of the HV lateral MOSFET, offering valuable insights into the device's physical characteristics.

Moving on, Fig. 4.4 showcases the simulated HV lateral MOSFET generated using sProcess, a simulation tool capable of accurately modeling and predicting the device's electrical
Figure 4.3: Schematic cross-sectional view of the HV Lateral MOSFET on N-epi/N+ substrate

Figure 4.4: Cross-section of the simulated HV lateral MOSFET using sProcess
behavior and performance characteristics. This simulation-based approach aids in gaining a comprehensive understanding of the device's operational dynamics, enabling effective design optimizations and performance enhancements.

Figure 4.5: Simulated electric fields of the HV Lateral MOSFET across the gate oxide (A-A') and along the P Well (B-B')

The critical design consideration of the lateral devices is to suppress the surface electric field and limit the critical electric field inside the semiconductor. Hence, in this work, the Al implanted P top region is used to reduce the surface electric field. Extensive 2D TCAD device and process simulations have been performed to optimize the device structure. The length and dose of the P top region are designed so that it completely depletes at the onset of reaching the critical electric field for avalanche breakdown. The positioning of the P top layer plays a role in determining the width of the junction field-effect transistor (JFET) region (L_JFET). Placing the gate poly-Si on the P top layer facilitates the field plate effect. The performance determines the lateral
device's blocking capability is directly influenced by the two dimensions: the length of the P top (L_{P\text{top}}) and the distance between the P top and the N+ drain (L_{gap}), which determine the source-to-drain length. Both the L_{P\text{top}} and L_{gap} dimensions are designed to ensure that the breakdown occurs inside the semiconductor suppressing the field in the oxide thereby avoiding oxide rupture.

Fig. 4.5 illustrates the simulated electric field profiles of the HV lateral MOSFET during the breakdown condition, focusing on two critical regions: the gate oxide (A-A') and the P Well (B-B'). The depicted electric field profiles reveal the deliberate design of the lateral MOSFET to effectively suppress the surface electric field to minimize potential surface breakdown effects and enhance the overall device performance, ensuring robust operation under high-voltage conditions. From Fig. 4.6a, it is evident that the L_{P\text{top}} cannot be too wide as the specific on-resistance (R_{on,sp}) increases linearly with its length. So, a reasonable length of p-top should be chosen to achieve the target BV. The dose of the P top should also be carefully optimized such that it does not completely deplete, which increases the electric field in oxide and hence reduces the breakdown voltage. From, Fig.4.6b the optimum dose of 1.8×10^{13} \text{ cm}^{-2} gives the highest BV. Similarly, the L_{gap} was optimized.

Figure 4.6: (a) Simulation results for the trade-off relation between BV and Ron for different lengths of P top (LP top) (b) Simulation results to optimize the dose in the P top

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in the same manner as the $L_{P\ top}$. The $L_{gap}$ needs to be wide enough to support the specified breakdown voltage while maintaining the low $R_{on,sp}$.

![Graph showing the trade-off relation between BV and Ron for different lengths of the gap ($L_{gap}$) between the P top and N+ drain](image)

**Figure 4.7:** Simulation results for the trade-off relation between BV and Ron for different lengths of the gap ($L_{gap}$) between the P top and N+ drain

It is critical to minimize the overall cell pitch to achieve the low $R_{on,sp}$, and still achieve a high blocking capability from the specified dimensions as discussed above. Based on the simulations, both the maximum breakdown voltage and the low $R_{on,sp}$ were accomplished when the P top (RESURF) dose is $1.8 \times 10^{13}$ cm$^{-2}$, the P top length ($L_{P\ top}$) is 4 μm, the P-top to drain gap ($L_{gap}$) is 1.5 μm. The cell pitch of the nominal device is 23.2 μm with a channel length ($L_{ch}$) of 0.5 μm.

**Table 4.1:** HV Lateral nominal MOSET design lengths

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Length (in μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length, $L_{ch}$</td>
<td>0.5</td>
</tr>
<tr>
<td>JFET, $L_{j fet}$</td>
<td>2</td>
</tr>
</tbody>
</table>

123
<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>P top, L_P top</td>
<td>4</td>
</tr>
<tr>
<td>L_gap</td>
<td>1.5</td>
</tr>
<tr>
<td>P+ Source</td>
<td>0.75</td>
</tr>
<tr>
<td>N+ Source</td>
<td>1.6</td>
</tr>
<tr>
<td>N+ Drain</td>
<td>2</td>
</tr>
</tbody>
</table>

The nominal design parameters of the HV nMOSFET are shown in Table 1. Fig. 4.9 shows the layout top view, schematic and layout cross-section of the HV lateral MOSFET. Fig. 4.9 shows the SEM cross-section of the fabricated HV lateral MOSFET with a multi-metal layered BEOL process.

Fig. 4.10 shows the typical on-wafer output characteristics and the extracted R_{on,sp} of the HV NMOS at 25°C and 200°C. The R_{on,sp} of HV NMOS at 25°C with gate-source voltage (Vgs) of 20 V and 25 V is 7.30 mΩ·cm² and 5.82 mΩ·cm², respectively. As shown in Fig. 4.11, the R_{on,sp}

**Figure 4.8:** (a) Top view of the nominal HV NMOS design (b) Cross-section of the HV NMOS (c) Layout view of the cross-section
increases with the rise in temperature due to the increase in the resistances of the drift layer, JFET region, and the interconnect metal layers.

**Figure 4.9:** SEM cross-section of the nominal HV lateral MOSFET

**Figure 4.10:** (a) The typical output characteristics of the fabricated lateral MOSFETs at room temperature. $V_{gs}$ of $0–25$ V is applied with $5$ V steps. Active area = $0.5$ mm$^2$ (b) Measured transfer characteristics ($V_{ds} = 0.1$ V) and transconductance of the lateral MOSFET, recorded at room temperature
Fig. 4.11 shows the transfer characteristics of the HV NMOS across temperature ranges up to 200°C and the extracted threshold voltage (Vth) at a drain-source current (Ids) of 100 μA is about 2.4 V at 25°C, adequate for power electronic applications. The Vth decreases with the increase in temperature. A negative threshold shift was observed, which can be attributed to the reduction in the voltage required for surface band bending (2Φf) for strong inversion.
increase in the intrinsic 4H-SiC carrier concentration ($n_i$) from room temperature to 300 °C and also the change in the charge ($Q_{IT}$) adhered in the interface states [23].

**Figure 4.13**: Blocking characteristics of the nominal HV NMOS measured at 25°C at $V_{gs}$ of 0V

Fig. 4.13 shows the typical forward blocking characteristics of the fabricated lateral HV MOSFETs. The breakdown voltage at a drain-source current of 100 μA is about 520 V for a gate-source voltage of 0V demonstrating a voltage-supporting capability of 104 V/μm in the lateral direction.

The development process of the HV lateral MOSFET involved the meticulous design of various critical parameters and multiple design variations. These essential aspects were thoughtfully incorporated into the mask set, ensuring a comprehensive and thorough exploration of the device's capabilities. In the subsequent sections, the output characteristics, blocking characteristics, and electrical trends observed in these devices are discussed.
4.2.2 High Current Lateral MOSFET

A substantially large HVN MOS with an active area of 4.3 mm$^2$ (other devices were 1.2 mm$^2$) is included to extract a large current. Figs. 4.14 and 4.15 show the typical output and blocking characteristics of the large current device.

**Figure 4.14:** The typical output characteristics of the large current device measured at 25°C

**Figure 4.15:** The typical forward blocking behavior of the large current device measured at 25°C
The large current device demonstrated a current capability of 10A and a blocking potential of 475V at a drain-source current of 100μA. The $R_{on,sp}$ of high current HV NMOS at 25°C with gate-source voltage (Vgs) of 20 V and 25 V is 8.21 mΩ·cm² and 6.91 mΩ·cm², respectively.

### 4.2.3 Variation in length of P top

P top is designed to reduce the surface electric field and thereby enhance the blocking capability. Lateral MOSFETs with various p-top lengths were designed.

Fig. 4.16 shows the output characteristics and Fig. 4.17 shows the blocking characteristics when the P top lengths are 2µm, 4µm, and 6µm. As evident, the BV increases from 400V to 580V as the $L_{P_{top}}$ length is increased from 3µm to 6µm. However, analyzing the trade-off plot (Fig. 4.18) this increase in BV comes with a trade-off, as the specific on-resistance exhibits a linear increase (from 5.07 mohm·cm² to 7.52 mohm·cm²) with the enlargement of the cell pitch. Consequently,

![Figure 4.16](image)

**Figure 4.16:** (a) The typical measured output characteristics of the HV lateral MOSFETs with varied P top lengths at (a) Vgs of 20V and (b) Vgs of 25V at room temperature
determining the optimal \( L_{\text{p\_top}} \) becomes crucial, requiring careful consideration of device and circuit requirements for various applications.

\[ \text{Figure 4.17: The blocking characteristics of the lateral HV NMOS when the length of the p-top is varied} \]

\[ \text{Figure 4.18: Measured trade-off between breakdown voltage and specific on-resistance when the length of p-top is varied} \]
### 4.2.4 Channel length variation:

The channel length was also varied to evaluate the impact of the channel resistance on the total resistance. Fig. 4.19 shows the typical output characteristics when the channel length is varied by 0.3µm, 0.4µm, and 0.5µm, at Vgs of 20V and 25V at 25°C.

![Output Characteristics](image)

**Figure 4.19:** (a) The typical measured output characteristics of the HV lateral MOSFETs with varied channel lengths at (a) Vgs of 20V and (b) Vgs of 25V at room temperature

Fig. 4.20 provides valuable insights into the performance characteristics of the HV lateral MOSFETs. The extracted specific on-resistance (Ron,sp) exhibits a notable reduction from 5.82 mohm-cm² to 4.33 mohm-cm² when the gate-source voltage (Vgs) is set at 25 V and the channel length is varied from 0.5 µm to 0.3 µm, respectively. This observation underscores the significant influence of channel resistance, validating its pivotal role as the dominant parameter in determining the overall resistance of the HV lateral MOSFETs.

Fig. 22 shows the blocking characteristics of the lateral MOSFETs with various channel lengths. The blocking voltage (measured at I<sub>ds</sub> of 100 µA) remains the same when the channel length is reduced to 0.4 µm from 0.5 µm (Fig. 4.20b). However, from the devices with a channel
length of 0.3 µm (Fig. 4.20a), a large leakage is observed at low drain voltages, which is attributed to a low potential barrier in the short channel. This is confirmed by the much-improved blocking behavior when a negative bias is applied between the gate and source (V\textsubscript{gs} = -5V). The device
blocks only 120V at Vgs of 0V but supports up to 420V when the channel is intentionally closed by applying a Vgs of -5V.

Fig. 4.21 shows the measured trade-off between breakdown voltage and specific on-resistance when the length of the channel is varied. From the trade-off, it is evident that channel resistance plays a dominant role and is a major contributor to the overall specific on-resistance of the devices.

### 4.2.5 Area efficient design variation

The SMART IC Lot 1 fabrication technology implemented a dual metal scheme. Utilizing the advantage of dual metal layers, source, and drain pads were placed on top of the active area to reduce the area occupied by the device. Fig. 4.22 shows the different layout design approaches.

**(a) Design A:** conventional layout design where pads are outside of the active area

**(b) Design B:** source and drain pads on top of the active area which reduces the area of the chip

**(c) Design C:** source and drain pads on top of the active area and gate pad incorporated into the source pad which further reduces the chip size from Design B

Figure 4.22: Design A is a conventional layout while Designs B and C use source and gate pads on the active area and gate pad incorporated into the source pad.
The blocking behavior of these three device designs is closely examined and the results are shown in Fig. 4.23. From Fig. 4.23, it is clear that the blocking capability of all three designs remains almost the same. Hence, design(c) can be greatly leveraged in future lots to include more devices by reducing the area currently occupied by the devices.

![Graph showing blocking behavior of three designs](image)

**Figure 4.23:** The blocking behavior of the designs (a) Nominal design (b) Source and drain pads on the active area (c) Source and gate pads on the active area and gate pad incorporated into the source

### 4.2.6 Metal 2 only on the pads

In this design, Metal 2 is used only on the pads while metal 1 runs along the fingers in the active area. This device was included to study the impact of the metal resistance on the overall resistance of the device. Since metal 2 is thicker than metal 1, using metal 2 only on the pads offers greater flexibility in designing devices with tighter cell pitch and reduces the overall specific on-resistances. Figs. 4.24 and 4.25 show the typical output and blocking characteristics of the HV MOSFET where metal 2 is present only on the pads. The specific on-resistance is slightly higher
Figure 4.24: Output characteristics of the HV MOSFET with metal 2 only on the pads

Figure 4.25: Blocking characteristics of the HV MOSFET with metal 2 only on the pads
(about 0.51mohm.cm² at Vgs of 20V) than the nominal device where metal 2 is present all along the active area. The blocking voltage, however, remains the same as nominal which is shown in Fig. 4.25.

4.2.7 PiN diode

Besides the MOSFETs, HV PiN didoes are designed using the same process steps. The forward conduction and blocking characteristics of the PiN diodes are discussed in this section. Fig. 4.26 shows the layout design of an HV PiN diode. Similar to HV NMOS, the voltage is supported by the p-top layer.

**Figure 4.26:** (a) Top view of the nominal HV NMOS design (b) Cross-section of the HV NMOS (c) Layout view of the cross-section
Figure 4.27: Forward voltage characteristics of the PiN diode measured at room temperature

Figure 4.28: Blocking behavior of the HV PiN diode with variation in the distance between P+ and P top
Fig. 4.27 shows the forward conduction and blocking characteristics of the HV PiN diode. The knee voltage of the PiN diode is around 2.7V when measured at 25 °C. The blocking capability of the PiN diode at a cathode current of 100μA is about 580V at room temperature as shown in Fig. 4.28.

4.2.8 Junction Barrier Schottky (JBS) diode

Fig. 4.29 presents the nominal layout design of an HV JBS diode. Similar to HV NMOS and PiN diodes, the voltage-supporting capability of the HV JBS diode is augmented by the presence of the p-top layer. Moving on to Figure 4.30, the forward voltage characteristics of the HV JBS diode are showcased.

Figure 4.29: (a) Top view of the HV JBS (b) Cross-section of the HV JBS (c) Layout view of the cross-section
It is noteworthy to observe that the knee voltage, which represents the onset of significant current flow, exhibits an anomalous value of approximately 2.5 V. This atypical behavior can be attributed to plasma-induced damage during the oxide etching process, specifically in the Schottky area of the diode. The plasma damage interferes with the desired Schottky behavior, resulting in the observed abnormal knee voltage.

**Figure 4.30:** Forward voltage characteristics of the HV JBS diode measured at room temperature (abnormal due to interface damage)

**Figure 4.31:** Forward voltage characteristics of the HV JBS diode measured at room temperature

**Figure 4.32:** Typical blocking characteristics of the JV JBS diode measured at room temperature

**Figure 4.33:** Typical blocking characteristics of the JV JBS diode measured at room temperature
Corrective measures have been diligently pursued in subsequent fabrication lots undertaken for other projects, involving different epitaxial doping profiles. Fig. 4.31 presents the forward voltage characteristics obtained from these subsequent lots, demonstrating the restoration of the appropriate Schottky behavior with a knee voltage that aligns with the expected values at 0.9V.

The blocking characteristics of the JBS diodes are depicted in Figs. 4.32 and 4.33, showcasing their impressive blocking capabilities. Both diodes exhibit remarkable voltage-blocking performance, with the first JBS (abnormal knee voltage) demonstrating a robust blocking capability at 580 V, while the second diode (corrected knee voltage) excels at a higher blocking voltage of 600 V. These results underscore the exceptional voltage-blocking characteristics inherent in the design and construction of the JBS diodes.

### 4.3 HV Lateral Devices on the N-epi/P-epi/N+ substrate

A fabrication process involving the utilization of a 2.5 µm thick n-epi layer, doped at a concentration of $6.5 \times 10^{16}$ cm$^{-3}$, in conjunction with a 6 µm thick p-epi layer, doped at a concentration of $2 \times 10^{16}$ cm$^{-3}$, on an N+ substrate was employed for the realization of the proposed high-voltage (HV) lateral Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and diodes. Precisely, nitrogen (N) and aluminum (Al) implantation techniques were employed to establish the N+ source/drain regions, P Well, P top, and P+ source regions, respectively. A unified process flow was employed to fabricate all the aforementioned devices, ensuring consistency and uniformity in the fabrication process.
4.3.1 Nominal HV lateral MOSFET design

Fig. 4.34 presents the schematic cross-section of the fabricated HV lateral MOSFET on the N-epi/P-epi/N+ substrate. Fig. 4.35 showcases the simulated HV lateral MOSFET generated using sProcess to accurately model and predict the device's electrical behavior and performance characteristics.

**Figure 4.34:** Schematic cross-sectional view of the HV Lateral MOSFET on N-epi/N+ substrate

The design and simulation methodology employed for the HV lateral MOSFET in this section adheres to the same principles and techniques utilized in the design of the previously reported HV lateral MOSFET fabricated on the N-epi/N+ substrate, as outlined in Section 4.2. As a result, a detailed discussion of the design techniques is not presented in this section, but instead, will be appropriately addressed and elucidated in subsequent sections, providing a comprehensive analysis of the design methodologies employed and their associated implications.
Figure 4.35: Cross-section of the simulated HV lateral MOSFET using sProcess

Table 4.2: Nominal parameters of the HV lateral MOSFET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Length (in μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length, $L_{ch}$</td>
<td>0.5</td>
</tr>
<tr>
<td>JFET, $L_{jefet}$</td>
<td>2</td>
</tr>
<tr>
<td>Ptop, $L_{ptop}$</td>
<td>4</td>
</tr>
<tr>
<td>$L_{gap}$</td>
<td>1.5</td>
</tr>
<tr>
<td>P+ Source</td>
<td>0.75</td>
</tr>
<tr>
<td>N+ Source</td>
<td>1.6</td>
</tr>
<tr>
<td>N+ Drain</td>
<td>2</td>
</tr>
</tbody>
</table>
The primary design consideration for the lateral devices revolves around the effective suppression of the surface electric field and containment of the critical electric field within the semiconductor structure. In this study, the utilization of an aluminum (Al) implanted P top region is implemented to effectively mitigate the surface electric field. To optimize the device structure, extensive 2D TCAD simulations, encompassing both device characteristics and fabrication processes, have been conducted. The dimensions and doping dose of the P top region are meticulously engineered to achieve complete depletion precisely when the critical electric field for

Figure 4.36: SEM cross-section the HV lateral MOSFET representing the N and P layers and the multi-metal layered BEOL process
avalanche breakdown is reached. The positioning of the P top layer assumes a pivotal role in determining the width of the JFET region, referred to as LJFET. By placing the gate poly-Si on the P top layer, the desirable field plate effect is facilitated, enhancing device performance.

The blocking capability of the lateral device, which is a crucial determinant of its overall functionality, is directly influenced by two key dimensions: the length of the P top region (L_{P\text{top}}) and the distance between the P top and the N+ drain (L_{gap}), which collectively determine the source-to-drain length. Careful consideration is given to both L_{P\text{top}} and L_{gap} dimensions, ensuring that the breakdown occurs within the semiconductor region, effectively suppressing the field in the oxide layer and thereby preventing oxide rupture.

![Diagram](a)

![Diagram](b)

**Figure 4.37:** (a) Top view of the nominal HV NMOS design (b) Cross-section of the HV NMOS and Layout view of the cross-section
The nominal design parameters of the HV lateral MOSFET are shown in Table. 4.2. Fig. 4.36 shows the SEM cross-section of the fabricated HV lateral MOSFET with a multi-metal layered BEOL process.

Fig. 4.37 shows the layout top view, schematic and layout cross-section of the HV lateral MOSFET. Fig. 4.38 shows the typical on-wafer output characteristics and the extracted $R_{on,sp}$ of the HV NMOS at 25°C and 200°C. The $R_{on,sp}$ of HV NMOS at 25 °C with gate-source voltage ($V_{gs}$) of 20 V and 25 V is 7.30 mΩ·cm² and 5.82 mΩ·cm², respectively.

Fig. 4.39 shows the transfer characteristics of the HV NMOS across temperature ranges up to 200°C and the extracted threshold voltage ($V_{th}$) at a drain-source current ($I_{ds}$) of 100 μA is about 2.4 V at 25°C, adequate for power electronic applications. The $V_{th}$ decreases with the increase in temperature. A negative threshold shift was observed, which can be attributed to the reduction in the voltage required for surface band bending ($2\Phi_f$) for strong inversion significant increase in the

**Figure 4.38:** (a)The typical output characteristics of the fabricated lateral MOSFETs at room temperature. $V_{gs}$ of 0 – 25 V is applied with 5V steps. Active area = 1.96mm²
intrin4H-SiC carrier concentration (n_i) from room temperature to 300 °C and also the change in the charge (Q_{it}) adhered in the interface states [23].

Figure 4.39: Transfer characteristics of HV NMOS at 25°C to 200°C

Figure 4.40: Blocking characteristics of HV NMOS measured at 25°C
Fig. 4.40 shows the typical forward blocking characteristics of the fabricated lateral HV MOSFETs. The breakdown voltage at a drain-source current of 100 μA is about 520 V for gate-source voltage of 0V demonstrating a voltage supporting capability of 104 V/μm in the lateral direction. Several critical parameters and design variations of HV MOSFET have been included in the mask set. Hence, the output characteristics, blocking behaviors, and trends of those devices are discussed hereafter.

### 4.3.2 High Current Lateral MOSFET

A substantially large HVN MOS with an active area of 4.3mm² is included to extract a large current. Figs. 4.41 and 4.42 shows the typical output and blocking characteristics of the large current device. The large current device demonstrated a current capability of 10A and a blocking potential of 475V at a drain-source current of 100μA.

![Figure 4.41](image)

**Figure 4.41:** The typical output characteristics of the large current device measured at room temperature
4.3.3 Variation in length of P top

Lateral MOSFETs with various p-top lengths were included to tailor the breakdown voltage. Fig. 4.43 shows the output characteristics when the p-top lengths are 2µm, 4µm, and 6µm.

Fig. 4.44 shows the blocking characteristics when the Ptop lengths are 3µm, 4µm, 6µm, and 8µm. As evident, the BV increases from 400V to 580V as the LTop length is increased from 3µm to 6µm. However, analyzing the trade-off plot (Fig. 4.45) this increase in BV comes with a trade-off, as the specific on-resistance exhibits a linear increase (from 6.4 mohm-cm² to 10.2 mohm-cm²) with the enlargement of the cell pitch. Consequently, determining the optimal LTop becomes crucial, requiring careful consideration of device and circuit requirements for various applications.

Figure 4.42: The typical forward blocking behavior of the large current device measured at room temperature.
Figure 4.43: (a) The typical measured output characteristics of the HV lateral MOSFETs with varied P top lengths at (a) Vgs of 20V and (b) Vgs of 25V at room temperature.

Figure 4.44: The blocking characteristics of the lateral HV NMOS when the length of the p-top is varied.
4.3.4 Channel length variation

The channel length was also varied to evaluate the impact of the channel resistance on the total resistance. Fig. 4.46 shows the typical output characteristics when the channel length is varied by 0.3µm, 0.4µm, and 0.5µm, at Vgs of 20V and 25V at 25°C.

Figure 4.46 provides valuable insights into the performance characteristics of the HV lateral MOSFETs. The extracted specific on-resistance ($R_{on,sp}$) exhibits a notable reduction from 6.88 mohm-cm² to 5.23 mohm-cm² when the gate-source voltage (Vgs) is set at 25 V and the channel length is varied from 0.5 µm to 0.3 µm, respectively. This observation underscores the significant influence of channel resistance, validating its pivotal role as the dominant parameter in determining the overall resistance of the HV lateral MOSFETs.
Figure 4.46: (a) The typical measured output characteristics of the HV lateral MOSFETs with varied channel lengths at (a) Vgs of 20V and (b) Vgs of 25V at room temperature

Figure 4.47: The blocking characteristics of the lateral HV NMOS when the length of the channel is varied

Fig. 4.47 shows the blocking characteristics of the lateral MOSFETs with various channel lengths. The blocking voltage (measured at $I_{ds}$ of 100 $\mu$A) remains the same when the channel length is reduced to 0.4 $\mu$m from 0.5 $\mu$m (Fig. 4.47b). However, from the devices with a channel length of 0.3 $\mu$m (Fig. 4.47a), a large leakage is observed at low drain voltages, which is attributed to a low potential barrier in the short channel. This is confirmed by the much-improved blocking...
behavior when a negative bias is applied between the gate and source ($V_{gs} = -5V$). The device blocks only 120V at $V_{gs}$ of 0V but supports up to 420V when the channel is intentionally closed by applying a $V_{gs}$ of -5V.

**Figure 4.48:** Measured trade-off relation between breakdown voltage and specific on-resistance when the channel length is varied

Fig. 4.48 shows the measured trade-off between breakdown voltage and specific on-resistance when the length of the channel is varied. From the trade-off, it is evident that channel resistance plays a dominant role and is a major contributor to the overall specific on-resistance of the devices.

### 4.3.5 Area efficient design variation

To pursue the half-bridge circuit, a major building block for the development of power electronic converters, there is a need for the integration of two power MOSFETs (high-side and low-side) on a single chip. This is feasible with no constraints only with the lateral architectural
devices. In vertical architecture, since the devices share the same substrate, multiple power MOSFETs operating at different voltages cannot be integrated on a single chip [4]. But, unlike vertical devices, due to their architecture, lateral devices inherently demand a larger cell pitch. So, any improvement in the cell pitch and chip size significantly impacts the development of high-performance economical devices and ICs. Hence, area-efficient HV lateral MOSFETs were designed for discrete device development as well as for monolithic integration in the HV Power IC applications. These area-efficient MOSFETs save a significant chip size allowing flexible cell design.

**Design A**

Fig. 4.49 shows the conventional layout view of the HV lateral MOSFET with drain, source, and gate pads. The corresponding SEM cross-section is shown in Fig. 4.50. The design implements interdigitated source and drain patterns. In Design A, all three metal layers are engaged over each of the source/drain fingers. Hence the drain, source, and gate metal pads are placed outside of the active area. This type of layout technique occupies a chip size of 3.32 mm². In this

![Design A layout top view: Chip size = 3.32mm², Active Area = 1.96mm²](image)

**Design B**

![Design B layout top view: Chip size = 2.50mm², Active Area = 1.84mm²](image)

**Design C**

![Design C layout top view: Chip size = 1.8mm², Active Area = 1.51mm²](image)

**Figure 4.49:** (a) Conventional design  (b) Source and drain pads on active (c) Source and gate pads on the active area and gate pad incorporated into the source
design, the cell pitch of the device is dictated by the critical dimension of the metal 3 (metal 3 - metal 3 spacing) as indicated in the layout cross-sectional view in Fig. 3. The metal 3 spacing between the source and drain should be mandatorily large (to avoid any electrical short) which consequently increases the cell pitch of the device and hence the $R_{on,sp}$.

**Designs B and C**

Employing the three metal layers BEOL process that was developed for the power IC technology, designs B and C were designed. Designs B and C overcome the shortcomings of the conventional Design A by placing the source and drain pads on the active area as shown in Figs. 4.49b and 4.49c. Although the designs still embrace the interdigitated source and drain patterns, the metal layers are not engaged over each other for every finger. The metal engagement for source and drain fingers is dictated by the top pad region. For example, at the source pad region, metals are not engaged with each other on the drain fingers and vice versa. Fig. 4.51 shows the SEM cross-sectional view of the devices with Designs B and C. Design B has a chip size of 2.5mm². In Design C, the chip area was further shrunk by incorporating the gate into the source pad achieving a chip size of 1.8mm² as shown in Fig. 4.49. Designs B and C significantly reduce the chip size when compared to Design A. Another significant advantage of Designs B and C when compared to Design A is, unlike Design A, the cell pitch of the devices with Designs B and C can be aggressively designed to reduce the cell pitch as there are no metal 3 source and drain interdigitated paths running across the layout.

The on-state characteristics of the HV lateral MOSFETs were measured at 25 °C and 200 °C. Fig. 4.52 shows the typical output characteristics of the HV lateral MOSFETs. Since the cell pitch of all the designs remains the same, the extracted $R_{on,sp, active}$ of the designs A, B, and C stay
similar at 6.2 mΩ·cm² at Vgs of 25V at 25 °C. The extracted $R_{on,sp,active}$ increases with the increase in temperature due to the increase in the JFET, drift, and metal resistances.

Figure 4.50: SEM cross-sectional view of Design A when cut across- A-A'

Figure 4.51: SEM cross-sectional view of Designs B and C when cut across B-B' and C-C' respectively
Figure 4.52: The typical output characteristics of designs A, B, and C at Vgs of 25V at 25 °C and 200 °C. Extracted $R_{on,sp,active}$ of the designs A, B, and C stay similar at 6.2 mΩ·cm² at Vgs of 25V and Vds of 0.1V at 25 °C.

Figure 4.53: The $R_{on,sp}$ comparison for all the three types of design variations; $R_{on,sp}$ extracted for both active area ($R_{on,sp,active}$) and chip size ($R_{on,sp,chip}$) at Vgs of 25V at 25 °C;
When contemplated the designs, the $R_{on,sp,active}$ for all three designs remain the same but the extracted $R_{on,sp,chip}$ of designs B and C are lower when compared to Design A due to their significant reduction in chip sizes as shown in Fig. 4.53. The reduction of $R_{on,sp,chip}$ leads to the implementation of designs B and C in developing area-efficient Power ICs. In addition, the blocking characteristics have also been evaluated. All three designs demonstrate a blocking capability of 430V in the lateral direction at $I_{ds}$ of 1mA at 25 °C as shown in Fig. 4.54. In designs B and C, it is imperative that the interlayer dielectric (ILD) between metal 1 and metal 3 should withstand a voltage that’s much larger than the breakdown voltage of the device since the source and drain metal lines crossover with each other as shown in Fig. 4.51. Hence, as shown in Fig. 5.5, when measured a MIM capacitor between metal 1 and metal 3, the 3.5μm ILD demonstrated a blocking capability of 1800V at 0.1nA validating the safe and robust operation of designs B and

![Figure 4.54: The blocking behavior of the Designs A: Nominal design, B: Source and drain pads on active area, C Source and gate pads on active area and gate pad incorporated into the source](image_url)
C. From Fig. 4.54, it is clear that the blocking capability of all three designs remains almost the same. Hence, design(c) can be greatly leveraged not only for the discrete device development but also to be implemented in the Power ICs.

4.3.6 Metal 3 only on the pads

In this design, Metal 3 is used only on the pads while metal 1 and 2 run along with the fingers in the active area. This device was included to study the impact of the metal resistance on the overall resistance of the device. Since metal 3 is thicker than metal 1 and 2, using metal 3 only on the pads offers greater flexibility in designing devices with tighter cell pitch and reduces the overall specific on-resistances. The cell pitch of this device is about 2.5μm smaller (20.7μm) than the nominal (23.2μm).

Figure 4.55: Output characteristics of the HV MOSFET with metal 2 only on the pads
Figure 4.56: Blocking characteristics of the HV MOSFET with metal 2 only on the pads

Figs. 4.55 and 4.56 shows the typical output and blocking characteristics of the HV MOSFET where metal 3 is present only on the pads. The specific on-resistance is slightly higher than the nominal device where all three metals are engaged and metal 3 runs all along the active area. The blocking voltage, however, remains the same as the nominal design.

4.4 BV-R\textsubscript{on,sp} trade-off performance of the reported HV Lateral MOSFETs

This section delves into an intricate analysis of the BV versus R\textsubscript{on,sp} trade-off performance exhibited by the HV lateral MOSFETs (Gen 1) developed in this study, comparing them to the extensively documented HV lateral MOSFETs reported in the literature [1]-[16]. Remarkably, as presented in Fig. 4.57, the superior capabilities of the lateral devices positioned them as best-in-class within the reported devices. The trade-off values of GaN normally-off HEMTs [17]-[22] are
also included for comparison. In Figure 4.57, the red and blue solid lines represent the hand calculations of 4H-SiC lateral and vertical MOSFETs, respectively, considering a channel mobility of 25 cm²/V-s (detailed in section 1.2.3 of this document).

These devices demonstrate not only a remarkable trade-off performance between BV and $R_{\text{on,sp}}$ but also possess the capability to handle substantial current levels, ranging from 5 to 10 A. These exceptional performance attributes can be attributed to the meticulous cell design, effective field management strategies, and refined peripheral designs that have been incorporated during the development of these devices.

**Figure 4.57**: BV-$R_{\text{on,sp}}$ trade-off plot capturing the performances of the 4H-SiC lateral devices reported in this work and the literature; the trade-off values of GaN normally-off HEMTs are also added; the red and blue solid lines represent the hand calculations of 4H-SiC lateral and vertical MOSFETs for channel mobility of 25 cm²/V-s
Given the outstanding performance displayed by HV lateral MOSFETs, there exists an opportunity for further improvement by incorporating innovative gate oxide recipes. These advancements can potentially elevate the performance of 4H-SiC lateral MOSFETs to a level comparable to that of 4H-SiC vertical MOSFETs. Consequently, 4H-SiC lateral MOSFETs could become formidable contenders in the 400-600V voltage range, effectively competing with gallium nitride high-electron-mobility transistors (HEMTs) in terms of specific on-resistance, breakdown voltage, HT performance, and reliability.

### 4.5 Next generation (Gen 2) HV Lateral MOSFET

#### 4.5.1 Issue and motivation for Gen 2 HV Lateral MOSFET

Although as highlighted in section 4.4, the superior performances of the HV lateral MOSFETs (Gen 1) of this work, these devices exhibited substantial leakage during their operation. Consequently, this study presents an improved design architecture for the HV lateral MOSFETs (Gen 2), which effectively addresses the leakage issue while simultaneously fulfilling the crucial design criterion of targeting the same breakdown voltage as our earlier design (Gen 1) to reduce losses during the blocking mode of operation.

The SEM and schematic cross-section of the Gen 1 HV lateral nMOSFETs are shown in Fig. 4.58. The Aluminum implanted P top region is employed to minimize the surface electric field while simultaneously amplifying the breakdown voltage of the device. The design of the P top (length and dose) is extremely critical in determining the blocking capability of the lateral device. The length of the P top for both conventional and proposed devices reported in this work is the same at 4μm. The dose of the P top region, in particular, should be carefully designed so that
Figure 4.58: Schematic and SEM cross-section of the Gen 1 HV Lateral MOSFET

Figure 4.59: Schematic and SEM cross-section of the Gen 2 HV Lateral MOSFET
it is not fully depleted leading to a significant increase in the electric field at the edge of the gate electrode. Although the designs are well optimized using the 2-D TCAD simulations, due to the process variations and incomplete ionization of the holes, the P top dose cannot be precisely controlled. Hence, the conventional design is susceptible to increasing the electric field at the edge of the gate and consequently increasing the leakage.

However, with the optimized new Gen 2 architectural design (Fig. 4.59), the proposed device thoroughly eliminates the shortcomings of the conventional device leading to enhanced performance in the blocking mode of operation. The SEM and the schematic cross-section of the proposed device with the new architecture are illustrated in Fig. 4.59. The new architecture incorporates a design where the gate is completely shielded and isolated from the P top. So, any process or uncontrollable dose variations in the p-top helps the gate current stay unaffected leading to low leakage during the blocking mode of operation.

Additionally, the Gen 2 architecture mitigates the prominent surface field management issues that commonly arise in lateral MOSFET designs. The gate-channel-JFET areas of the Gen 2 design bear a striking resemblance to those of vertical MOSFETs, which enables the application of similar techniques to enhance field management, reliability, and ruggedness. As a result, this novel architecture presents an excellent solution for the design of lateral MOSFETs. Through further optimization, the proposed device's cell pitch can be reduced when compared to a conventional device. Figs. 4.60a and 4.60b depict the simulated cross-sections and the corresponding electric field profiles along the gate for Gen 1 and Gen 2 HV nMOSFETs, respectively. As seen in Fig. 4.61, the Gen 1 device shows a larger electric field at the edge of the gate while in the Gen 2 device, the electric field is greatly reduced along the gate and across the gate oxide (A-A').
Figure 4.60: Simulated electric fields of the Gen 1 HV lateral nMOSFET and the (b) simulated electric field cross-section of the Gen 2 HV lateral nMOSFET.

Figure 4.61: Simulated electric field profiles of the Gen 1 and Gen 2 devices of HV lateral MOSFETs at the breakdown; the Gen 1 device shows a large electric field raise at the edge of the gate electrode while the electric field in the Gen 2 device is greatly suppressed.
**Figure 4.62:** Measured gate-source current for the Gen 1 and Gen 2 devices; the Gen 1 device shows the increase in the gate current with the increase in the drain-source voltage while the proposed device remains unaltered.

**Figure 4.63:** Measured drain-source current for the Gen 1 and Gen 2 devices; the Gen 1 device shows the increase in the drain-source current due to the increase in the gate-source current with the increase in drain-source voltage.
The measured gate-source leakage from the conventional and the proposed devices are shown in Fig. 4.62. The gate current from the conventional device significantly increases as the charges in the P top are depleted with the increase in the drain voltage while the gate current from the proposed device remains unaltered. Fig. 4.63 shows the measured drain-source leakages from the conventional and proposed HV nMOSFETs. As anticipated, due to the gate-source leakage the overall drain-source leakage increases for the conventional device but it remains the same across the voltage range for the proposed devices. Hence, the results demonstrate that the proposed device design for the lateral nMOSFET is effective in suppressing the gate leakage current and providing enhanced performance by suppressing the leakage as compared to the conventional design.

The critical dimensions to improve the breakdown voltage of the proposed HV lateral nMOSFETs are to vary the length of the P top \( L_{\text{P top}} \) and the gap between the p-top and the N+

![Graph](image)

**Figure 4.64:** The typical forward blocking behavior of the lateral MOSFET with proposed device design and variation in the \( L_{\text{gap}} \) of the MOSFET; the blocking capability of 700 V is demonstrated at the drain current of 100μA and \( V_{gs} = 0 \) V
Increasing the $L_{\text{P\,top}}$ or $L_{\text{gap}}$ increases the distance between the source and drain facilitating an effective distribution of electric field leading to enhancement in the breakdown voltage. However, the cell pitch of the device will be linearly increased with the increase in the dimensions of $L_{\text{P\,top}}$ or $L_{\text{gap}}$. Hence, in this work, with a deviation from the nominal parameters ($L_{\text{P\,top}} = 4\,\mu\text{m}$ and $L_{\text{gap}} = 1.5\,\mu\text{m}$), utilizing the proposed device design, a variation in the increase ($1.5\,\mu\text{m}$ to $2.5\,\mu\text{m}$) in $L_{\text{gap}}$ resulted in a breakdown voltage as high as 700V at a drain-source current of 100 $\mu\text{A}$ demonstrating a voltage-supporting capability of 107.6 V/µm in the lateral direction as shown in Fig. 4.64.

4.6 Conclusions

This chapter focused on the development of HV Lateral MOSFETs and diodes operating at (400V - 600V) in 4H-SiC, specifically tailored for integration within power ICs. The development process included 2D sDevice and sProcess simulations and in-depth analysis of experimental results. The HV lateral devices were fabricated on N-epi/N+ substrates and N-epi/P-epi/N+ substrates, leading to designing the best-in-class BV - $R_{\text{on,sp}}$ trade-off performances. Not only that the devices have the best trade-off performance, but they are also high current rated (5A - 10A) which demonstrates the design and edge termination efficiency. A notable accomplishment is the demonstration of an enhanced design architecture (Gen 2) for lateral devices in 4H-SiC which addresses all the prominent surface field management issues in lateral devices making it a robust and reliable design.
4.7 References


CHAPTER 5: Isolation Techniques for the HV Power IC Technology

5.1 Introduction

The need for high voltage isolation in power IC technology arises from the requirement to ensure the safety, reliability, and proper functioning of electronic systems. High voltage isolation is necessary to prevent electrical leakage and isolate sensitive circuitry from potentially high voltage levels. In high-voltage power ICs, where high voltages are present, proper isolation techniques are crucial to address these concerns and enable the development of efficient and reliable power systems. Isolation techniques create a barrier between high-voltage and low-voltage regions, preventing electrical current flow while allowing for signal transmission or power transfer. Various isolation techniques have been developed to address the isolation needs in high voltage power ICs, each with its advantages and considerations [1]-[10].

On-chip isolation techniques play a crucial role in high-voltage power IC technology by providing electrical isolation between different voltage domains on the same chip. These techniques allow for compact integration, reduced system complexity, and improved overall performance. Some of the widely used on-chip isolation techniques are silicon dioxide (SiO2) isolation, commonly known as shallow trench isolation (STI), deep trench isolation, p-n junction isolation, which relies on the formation of reverse-biased p-n junctions, silicon-on-insulator (SOI) technology have been employed in high-voltage power ICs where a thin layer of silicon on top of a buried insulating layer, typically SiO2 or sapphire.

Junction isolation and trench oxide isolation have been the most prominently used isolation techniques in WBG-based (GaN and 4H-SiC) power ICs [11]-[20].
5.2 Junction Isolation versus Trench oxide Isolation

**Junction Isolation**

Junction isolation involves the creation of isolation regions by forming p-n junctions around the active device regions. These junctions act as barriers, preventing the flow of electrical current between different regions. One of the key advantages of junction isolation is its simplicity and compatibility with standard CMOS processes [1]. Junction isolation provides enhanced electrostatic discharge (ESD) protection [1]. The presence of p-n junctions in junction isolation structures enables efficient dissipation of electrostatic charges and provides a robust ESD protection mechanism. The diode-like behavior of the junction facilitates the diversion of excessive charges away from sensitive circuitry, thereby safeguarding the integrity and reliability of the high-voltage power IC. In comparison, deep trench oxide isolation may require additional ESD protection structures or techniques to achieve comparable levels of protection [7]. Junction Isolation provides moderate immunity to noise when compared to oxide Isolation.

**Trench Oxide Isolation**

Trench oxide isolation involves the formation of deep and narrow trenches that are filled with insulating materials such as silicon dioxide (SiO₂). Trench oxide isolation provides excellent electrical isolation by physically separating different regions on the chip [1], [2], [6]-[8]. One of its advantages over junction isolation is its superior isolation performance and higher breakdown voltage. The trench structure offers a larger distance between the isolated regions, enabling higher voltage to withstand capabilities and minimizing the risk of electrical breakdown. Furthermore, deep trench oxide isolation provides improved isolation from noise and interference. The trench oxide structure acts as a physical barrier, preventing the coupling of electrical noise between
different regions of the chip. This isolation from noise sources enhances the signal integrity and overall performance of the high-voltage power ICs, making them suitable for applications that require high immunity to noise.

5.3 Junction isolation adoption in SMART IC technology

As studied in the previous sections, both junction isolation and deep trench oxide isolation are two widely used techniques and both have their significant share of advantages in achieving isolation for HV power IC technology. Junction isolation offers advantages such as simplicity, compatibility with CMOS processes, scalability, and cost-effectiveness. While the deep trench oxide isolation on the other hand offers superior isolation performance, higher breakdown voltage, improved noise isolation, and enhanced thermal dissipation. However, in developing the HV Power ICs in this SMART IC technology, junction isolation has been adopted due to its feasibility, cost-effectiveness, and seamless compatibility with the process flow. Fig. 5.1 shows the schematic cross-section showing the monolithic integration of HV lateral MOSFET, and LV CMOS on a single chip by implementing P+ Isolation implanted regions to isolate the HV and LV blocks. Fig. 5.2 shows the captured SEM cross-section of the P+ Isolation implanted region.

The P+ Isolation is 2.5μm deep and was implemented by channeling implantation (0 deg., normal to [0001]). The P+ Isolation in conjunction with the bottom P- epi layer is used to isolate the potential of the N-epi with another. When measured the voltage differential across two N-epi regions, the P+ Isolation shows a blocking capability of 320V as shown in Fig. 5.3, justifying the effectiveness of the P+ Isolation region.
Figure 5.1: Schematic cross-section showing the monolithic integration of HV lateral MOSFET, LV CMOS on a single chip by implementing P+ Isolation implanted regions to isolate the HV and LV blocks.

Figure 5.2: SEM cross-section of the P+ Isolation region implemented using channeling implantation.
In high-voltage power IC technology, the need for metal-to-metal interlayer dielectric (ILD) voltage blocking capability arises from the requirement to provide electrical insulation and prevent electrical breakdown between adjacent metal layers carrying different voltage potentials. [1], [2], [4]-[6]. ILD serves as the dielectric material between metal layers, and its voltage-blocking capability is essential for ensuring the reliable and safe operation of high-voltage power ICs. High-voltage power ICs often involve multiple metal layers that carry distinct voltage potentials, such as high-voltage power supply lines, signal lines, or control lines. The ILD material, typically silicon dioxide (SiO$_2$) or other insulating materials, provides a critical electrical barrier between these metal layers, preventing unintended electrical coupling or short circuits. The voltage-
blocking capability of the ILD ensures the isolation and integrity of different voltage domains, minimizing crosstalk and maintaining the proper functioning of the circuitry.

In the SMART IC technology, efforts have been dedicated to designing the ILD (thickness) so that the metal-to-metal interlayer dielectric (ILD) voltage blocking capability is high so that the power IC technology is driven to address the requirements of electrical isolation, protection of sensitive components, reduction of leakage current and parasitic capacitance, and overall reliability.

![SEM cross-section](image.png)

**Figure 5.4:** SEM cross-section reveals the characteristic metal layers with the ILD material sandwiched in between

The voltage-blocking capability of the interlayer dielectric (ILD) material is assessed through the application of a voltage across a metal-insulator-metal (MIM) capacitor. Two MIM capacitors are evaluated, with one located between Metal 1 and Metal 2, and the other between Metal 2 and Metal 3. The SEM cross-section (Fig. 5.4) reveals the characteristic metal layers with the ILD material sandwiched in between. The ILD thickness between Metal 1 and Metal 2 measures approximately 1.5 μm, while the thickness between Metal 1 and Metal 3 is around 4.5 μm.

Fig. 5.5 illustrates the voltage-blocking capabilities of the MIM capacitors. The ILD material demonstrates a high breakdown field, as evidenced by its blocking voltage of
approximately 900V between Metal 1 and Metal 2, and 2000V between Metal 1 and Metal 3. This high breakdown field exhibited by the ILD material establishes its suitability and reliability for the development of power-integrated circuits (ICs).

![Breakdown field plots](image)

**Figure 5.5:** Blocking capability of the ILD measured from a MIM capacitor between (a) metal 1 and metal 2 (b) metal 1 and metal 3

### 5.5 Conclusions

This chapter delved into high-voltage isolation techniques crucial for ensuring the safety, reliability, and proper functioning of electronic systems. Various techniques to prevent electrical leakage and isolate sensitive circuitry from damaging voltage levels are discussed, with specific emphasis on junction isolation using the P+ Isolation junction implemented by channeling implantation for the SMART IC development. The effectiveness of these techniques is supported by electrical measurements. Furthermore, the interlayer dielectric (ILD) voltage-blocking capability for metal-to-metal insulation between different voltage potentials is addressed, evaluating the ILD blocking capabilities between metals.
5.6 References


CHAPTER 6: Edge Termination Techniques for 4H-SiC Lateral Power Devices

6.1 Introduction

Edge termination refers to the design and implementation of structures and techniques at the edges of semiconductor power devices to control and distribute the electric field, thereby improving the breakdown voltage and ensuring reliable operation. Power devices, such as power MOSFETs, IGBTs (Insulated Gate Bipolar Transistors), and diodes, operate at high voltages and currents, making them prone to electric field concentration and premature breakdown at the device edges. Edge termination design plays a critical role in mitigating these effects and enhancing device performance and reliability.

The need for edge termination design in power devices arises from several factors. One of the primary concerns is the electric field crowding effect that occurs near the edges of the active device area. In power devices, the electric field distribution is not uniform across the entire device structure. The electric field tends to concentrate near the edges, leading to higher electric field intensities and potential breakdown points. Edge termination design aims to distribute the electric field more evenly, reducing the electric field crowding effect and enhancing the voltage-blocking capability of the device [1]-[4]. Moreover, edge termination design plays a crucial role in preventing edge breakdown and surface leakage currents. The edges of power devices are prone to surface imperfections, such as crystal defects, contaminants, or roughness, which can create localized electric field enhancements and initiate electrical breakdown. By utilizing appropriate edge termination techniques, such as field plates, guard rings, or junction termination extensions, the electric field is gradually tapered and distributed along the device periphery, reducing the risk.
of edge breakdown and minimizing surface leakage currents [1]-[4]. Additionally, edge termination design is also necessary to reduce the sensitivity of power devices to external influences, such as surface contamination, humidity, or temperature variations. By employing appropriate edge termination structures and materials, the electric field distribution at the edges can be stabilized, making the device less susceptible to environmental factors that could lead to device performance degradation or electrical failures. The edge termination design enhances the robustness and long-term stability of power devices, enabling them to withstand harsh operating conditions [1]-[4]. In conclusion, edge termination design is crucial for power devices, especially those with high voltage ratings, to ensure reliable operation and prevent premature breakdown. By addressing electric field crowding, reducing edge breakdown risks, extending the voltage-blocking region, and enhancing device robustness, edge termination design plays a significant role in achieving high-performance power devices for various applications.

Various methods are employed, including field plate termination, resistive termination, bevel termination, floating field rings (FFRs), and junction-termination-extension (JTE) [5]-[8]. Among these techniques, FFR and JTE have gained prominence in the context of 4H-SiC devices. However, FFR implementation poses manufacturing challenges due to the requirement for precise lithography patterning to define a narrow critical dimension between the PN main junction and the initial P+ concentric ring, essential for achieving a high breakdown capability. In recent years, JTE-based edge termination structures have emerged as viable alternatives.

In contrast to vertical devices, the requirement for edge termination in lateral devices is contingent upon the chosen layout technique. Therefore, this chapter delves into a thorough exploration of the methodologies employed to manipulate the electric field in lateral devices, both with and without edge termination, with the objective of enhancing the breakdown voltage.
Detailed discussions on these techniques shed light on their effectiveness and implications in achieving improved device performance.

6.2 Interdigitated layout technique

In contrast to vertical MOSFETs, the layout design of lateral devices prominently utilizes interdigitated patterns due to the positioning of the source, gate, and drain pads on the device's top surface. The interdigitated layout technique plays a crucial role in enhancing the performance of lateral devices, offering advantages such as improved current handling, enhanced thermal management, and reduced parasitic effects [15].

![Figure 6.1](image)

**Figure 6.1:** (a) Schematic top-view layout of the drain-centered design layout and (b) schematic top-view layout of source-centered layout design
In terms of blocking capabilities, the interdigitated layout technique is beneficial as it distributes the electric field more effectively. This helps to mitigate field crowding effects and improves the BV performance of lateral devices [4].

Fig. 6.1 illustrates two distinct outcomes resulting from interdigitated source-drain patterns, each exhibiting unique characteristics. The first outcome, as depicted in Fig. 6.1a, pertains to the drain-centered design, wherein the drain is positioned on the inner side while the source resides on the outer side. Conversely, the second outcome (Fig. 6.1b) corresponds to the source-centered design, where the drain is located on the outer side.

Figure 6.2: (a) Schematic top-view layout of the drain-centered design layout and (b) schematic top-view layout of source-centered layout design

Fig. 6.2a illustrates the cross-section of the HV lateral MOSFET, while Fig. 6.2b showcases the electric field distribution within the lateral device during breakdown. As anticipated, Fig. 6.2b indicates that the electric field at the drain region reaches zero, while it remains high at the bottom.
of the P Well/N-epi junction. Consequently, as depicted in Figure 6.1b, if the layout is structured such that the drain is positioned on the outer side, the necessity for any form of edge termination is obviated. However, if the source is located on the outer side, conventional edge termination techniques like JTE-based or floating field rings (FFR) can be employed to achieve effective termination. So, subsequent sections in this chapter delve into a comprehensive simulation analysis of edge termination techniques specifically designed for drain-centered layouts. The efficacy and performance of these techniques are then subjected to thorough experimental verification and validation, ensuring their effectiveness and functionality in peripheral designs.

6.3 Edge termination designs for drain-centered layouts

A vertical PiN diode constructed on a 6 μm, 2.4e16 cm⁻³ doped N-epi/N+ substrate is considered to perform simulations and optimize the edge termination techniques for the drain-centered designs. This section provides an in-depth analysis of various edge termination techniques, offering a concise introduction to each technique along with extensive simulations aimed at optimizing the relevant parameters.

6.3.1 Single Zone - Junction Termination Extension (SZ-JTE)

The single zone JTE edge termination design works based on the principle of extending the space charge region and redistributing the electric field lines away from the edges of the device. This is achieved by introducing a lightly doped region, often with a lower doping concentration compared to the active device region, near the device periphery. The JTE acts as an extension of the active device junction, effectively increasing the length of the depletion region and providing a gradual transition of the electric field towards the edges of the device [1]-[5].
Figure 6.3 presents a cross-sectional view of the device featuring two different structures: one without edge termination and another incorporating a single zone-junction termination extension (SZ-JTE).

![Schematic cross-sectional view of P+/N- junction](image)

**Figure 6.3:** Schematic cross-sectional view of P+/N- junction (a) without edge termination and (b) with SZ-JTE structure.

Simulations reveal that (Fig. 6.4), in the structure with no edge termination structure creates a sharp electric field peak at the end of the P+ junction, resulting in a premature breakdown voltage of 300 V. However, with the inclusion of the SZ-JTE next to the P+ junction, the electric field is
effectively distributed across the JTE area, significantly enhancing the voltage-supporting capability to an up to 850V.

The performance of the single-zone junction-termination-extension (SZ-JTE) technique relies on the dimensions and implant dose of the JTE (P-) region. To extend the horizontal depletion layer, it is recommended to have a JTE region width that is at least 3 to 5 times the thickness of the drift layer [16]. The breakdown voltage of the device is determined by the implant dose of the JTE region, as depicted in Fig. 6.5. The results indicate that a low JTE dose (below $1.7 \times 10^{13}$ cm$^{-2}$) leads to a low breakdown voltage, while a high JTE dose (above $1.9 \times 10^{13}$ cm$^{-2}$) causes the JTE region to become highly concentrated and effectively extends the P+ main junction.

**Figure 6.4:** Simulated electric field across A-A’ with no Edge Termination (ET) and with SZ JTE
From simulation results (Fig. 6.5), the ideal JTE dose for achieving the highest breakdown voltage is found to be $1.8 \times 10^{13}$ cm$^{-2}$. However, it is difficult to accomplish the targeted dose due to process variations and also due to incomplete activation of the implanted dopants [17]-[19] which might reduce the BV from the targeted value. To address this challenge, the Ring Assisted-JTE (RA-JTE) technique is pursued as a solution.

6.3.2 Ring Assisted - Junction Termination Extension (RA-JTE)

To address the sensitivity of the dose in the SZ-JTE, a solution called Ring Assisted (RA) - Junction-Termination-Extension (JTE) has been introduced. By incorporating a P+ floating ring within the single-zone JTE (SZ-JTE) structure, the electric field at the P+ main junction can be effectively reduced, especially for lower JTE doses compared to the optimal dose [20]. This approach significantly widens the process window and resolves the sensitivity issues associated
with the SZ-JTE structure. The schematic cross-sectional view of the RA-JTE structure is depicted in Fig. 6.6.

![Schematic cross-sectional view of RA-JTE structure](image)

**Figure 6.6:** Schematic cross-sectional view of P+/N- junction with RA-JTE

![Simulated breakdown voltage vs. JTE dose](image)

**Figure 6.7:** Simulated breakdown voltage as a function of JTE dose using RA-JTE

The design of the RA-JTE structure requires optimization of the initial spacing between the first floating P+ ring and the main junction (S₀) as well as the incremental spacing between subsequent floating rings (Sᵢ). The placement of the RA-JTE structure follows the equation:
\[ S_n = S_0 + S_i(n-1), \]

where \( S_n \) represents the corresponding spacing based on the number of rings, \( S_0 \) is the initial spacing of the ring from the main P+ junction, \( S_i \) is the incremental spacing of the ring, and \( n \) is the number of rings.

**Figure 6.8:** Simulated electric field profile across A-A’ for the structure with RA-JTE

Through simulations, it was optimized that the RA-JTE with \( S_0 \) of 1 \( \mu \text{m} \), \( S_i \) of 0.25 \( \mu \text{m} \), and \( n \) of 4 are required to target the ideal breakdown voltage. Fig. 6.7 illustrates the simulated breakdown voltage of the SZ-JTE and the optimized RA-JTE as a function of the JTE dose. The RA-JTE demonstrates a wider process window at lower doses, enabling the achievement of higher breakdown voltage compared to the SZ-JTE through the utilization of P+ floating rings within the JTE structure. Fig. 6.8 shows the simulated electric field profile at the breakdown of the RA-JTE across A-A’ (Fig. 6.6).
6.3.3 Multiple Floating Zone - Junction Termination Extension (MFZ-JTE)

The MFZ-JTE structure is designed to address the limitations of the SZ-JTE at higher JTE doses [20]-[23]. In the MFZ-JTE structure, multiple floating zones are implemented around the active device region. These zones are lightly doped regions that are electrically isolated from each other and the active device area. The purpose of these floating zones is to redistribute the electric field along the periphery of the device, effectively mitigating electric field crowding near the edges and enhancing the voltage-blocking capability.

Fig. 6.9 illustrates a schematic cross-sectional view of the MFZ-JTE structure, highlighting its configuration. The charge distribution within each zone of the MFZ-JTE structure is achieved through a single ion implantation process. By controlling the width of the discrete JTE region, the effective charge or dose within the structure can be precisely regulated. The width of the JTE zones decreases as the number of discrete zones increases, employing a decreasing parameter $\alpha$. This approach facilitates a gradual distribution of charge across the MFZ-JTE design, ensuring optimized performance. To design the MFZ-JTE edge termination, the width of the JTE zones can be adjusted using the following equation:

$$W_n = \frac{W_1}{\alpha^{(n-1)}}$$

This equation allows for fine-tuning of the JTE zone width ($W_n$), enabling efficient control over the charge distribution within the MFZ-JTE structure.

$W_n$ is the JTE width of the $n^{th}$ zone, $W_1$ is the first JTE width, $\alpha$ is the decreasing parameter, and $n$ is the number of the zone.
Fig. 6.10 illustrates the simulated breakdown voltage of the SZ-JTE, RA-JTE, and MFZ-JTE structures as a function of the JTE dose. Below the optimum dose ($1.8 \times 10^{13}$ cm$^{-2}$), the MFZ-JTE structure exhibits blocking characteristics similar to those of the SZ-JTE structure. Insufficient charge in the MFZ-JTE zones hinders the mitigation of the high electric field at the P+ main junction, mirroring the behavior of the SZ-JTE structure.

However, when the JTE dose surpasses the optimum level ($1.8 \times 10^{13}$ cm$^{-2}$), the MFZ-JTE structure demonstrates high breakdown voltages by effectively distributing the electric field across each zone, as depicted in Fig. 6.11. This distribution reduces the electric field at the JTE region's edge. The gradual charge distribution of the JTE zones within the MFZ-JTE structure plays a vital role in achieving high breakdown voltages at higher JTE doses. Consequently, the MFZ-JTE structure offers an increased process window, allowing for greater flexibility and enhanced performance.

**Figure 6.9:** Schematic cross-sectional view of P+/N- junction with MFZ-JTE

![Schematic cross-sectional view of P+/N- junction with MFZ-JTE](image-url)
Figure 6.10: Simulated breakdown voltage as a function of JTE dose using MFZ-JTE

Figure 6.11: Simulated electric field profile across A-A’ for the structure with MFZ-JTE
6.3.4 Hybrid - Junction Termination Extension (Hybrid-JTE)

Based on the findings presented in the preceding sections, it is clear that the RA-JTE structure facilitates the attainment of high breakdown voltages at lower JTE doses, whereas the MFZ-JTE design expands the process latitude for higher JTE doses. Therefore, by capitalizing on the strengths of both RA-JTE and MFZ-JTE, it is possible to create a Hybrid-JTE configuration by incorporating the MFZ-JTE adjacent to the RA-JTE structure [20]-[22]. Fig. 6.12 depicts a schematic cross-sectional view of the Hybrid-JTE edge termination structure, illustrating the integration of both RA-JTE and MFZ-JTE elements.

**Figure 6.12:** Schematic cross-sectional view of P+/N- junction with Hybrid-JTE

Fig. 6.13 illustrates the simulated breakdown voltage as a function of the JTE dose, wherein the SZ-JTE, RA-JTE, and MFZ-JTE structures are provided as reference points. Additionally, Fig. 6.14 showcases the simulated electric field distribution for the Hybrid-JTE structure at JTE doses of $(1.5 \times 10^{13} \text{ cm}^{-2})$ (low dose case) and $2.5 \times 10^{13} \text{ cm}^{-2}$ (high dose case). Upon examination, it is evident that the RA-JTE component primarily supports the electric field in the low dose case, while
Figure 6.13: Simulated breakdown voltage as a function of JTE dose using SZ, RA, MFZ, and Hybrid-JTE

Figure 6.14: Simulated electric field profile across A-A’ for the structure with Hybrid-JTE
the MFZ-JTE component effectively manages an enhanced electric field in the high-dose case, resulting in high breakdown voltages throughout the entire range.

To summarize, the Hybrid-JTE edge termination technique offers a substantial process latitude for the JTE dose, allowing for fabrication without being excessively impacted by variations in JTE dose and activation ratio in 4H-4H-SiC power devices. Consequently, for drain-centered designs, the Hybrid-JTE method was employed in this work as a highly effective termination technique.

6.3.5 Floating Field Ring (FFR) Edge Termination

The utilization of a floating field ring (FFR) or guard ring edge termination structure is appealing due to its elimination of additional masking and implantation steps, which are typically required in JTE-based edge termination techniques [20]-[22].

![Figure 6.15: Schematic cross-sectional view of P+/N- junction with FFR](image)

By employing the same processing step used to form the P+ main junction for the PN diode and the P+ contact for the MOSFET, the formation of P+ floating rings can be accomplished simultaneously, as depicted in Fig. 6.15. To effectively mitigate the high electric field at the main
junction, the FFR structure requires a narrower minimum feature size compared to the RA-JTE structure, presenting challenges in defining the critical dimension during the manufacturing process. Similar optimization techniques employed for RA-JTE have been applied to FFR structures. Fig. 6.16 demonstrates the successful termination of targeted breakdown voltages using FFR for effective termination.

![Simulated electric field profile across A-A’ for the structure with FFR](image)

**Figure 6.16:** Simulated electric field profile across A-A’ for the structure with FFR

### 6.4 Edge termination and Peripheral designs of HV lateral MOSFETs — experimental demonstration

An effective cell and peripheral design, simplified process for integration, smaller footprint, and superior performance are inevitable expectations from the HV Lateral MOSFET for the development of HV Power ICs. This section delves into the study of the performance of the drain-centered and source-centered techniques for the HV lateral MOSFETs by experimental
verification. This study ensures the effectiveness and functionality of the peripheral designs. The results from the HV lateral MOSFETs that were fabricated on both 6” N-epi/N+substrate and N-epi/P-epi/N+substrates for the development of the Power ICs were reported. The different lateral HV nMOSFET designs that were fabricated and reported in this work are summarized in Fig. 6.17. The top view schematics of the drain-centered design and source-centered design with and without the P+ Isolation are shown in Figs. 6.18, 6.19, and 6.20, respectively.

**Figure 6.17:** Summary of the lateral HV NMOS devices fabricated on six-inch N-epi/N+ substrate and N-epi/P-epi/N+ substrates
Figure 6.18: Top view schematic of the drain-centered design with Hybrid JTE termination

Figure 6.19: Top view schematic of the source-centered design

Figure 6.20: Top view schematic of the source-centered design with the P+ Isolation junction termination
6.4.1 HV Lateral MOSFETs on N-epi/N+ substrate

Fig. 6.21 shows the cross-sections of the lateral HV nMOSFET on N-epi/N+substrate with drain-centered (P+source outside) and source-centered (N+drain outside) designs.

**Figure 6.21:** (a) Drain-centered design where the P+ source is on the outside and Hybrid-JTE is used to terminate the electric field; (b) Source-centered design where the N+ drain is on the outside and no termination required.

The simulated electric field profile at breakdown across A-A’ shows the effective distribution of electric field by the Hybrid JTE termination in Fig. 6.22a. For source-centered design, since the N+ drain is on the outside, the electric field at the breakdown is ceased inside the device, as shown in Fig. 6.23a, eliminating the demand for edge termination. Since the active area
of both the devices is the same, the corresponding $R_{\text{on,sp}}$ of HV nMOSFET at a gate-source voltage ($V_{gs}$) of 25 V remain identical at 5.42 and 5.48 m$\Omega$·cm$^2$ at 25 °C, as shown in Fig. 6.22b and 6.23b. Both the drain-centered and source-centered designs on N-epi/N+substrate also demonstrate a similar blocking capability of ~520 V at $V_{gs}$ of 0 V validating a voltage supporting capability of 104 V/µm in the lateral direction, as shown in Figs. 6.22c and 6.23c.

**Figure 6.22**: (a) Electric field profile across A-A’ at the breakdown (b) Typical output characteristics and the extracted $R_{\text{on,sp}}$ at $V_{gs}$ of 25 V and $V_{ds}$ of 0 (c) Blocking characteristics measured at 25°C
6.4.2 N-epi/P-epi/N+ substrate

For the development of HV Power ICs, the isolation of HV and LV blocks is essential, which is missing in the N-epi/N+substrate, as all the devices share the same N+ conducting substrate. Hence, a bottom P-epi is necessary between N-epi and N+ substrate which offers the isolation using techniques such as junction isolation, and trench oxide isolation [24], [25]. A >2.5
Figure 6.24: Drain-centered design where the P+ source is on the outside and Hybrid-JTE is used to terminate the electric field; (b) Source-centered design with and without P+ isolation.

\( \mu \)m thick P+ junction isolation implemented by channeling implantation (0 deg., normal to [0001]) was adopted to isolate the HV and LV devices in this work. This P+ isolation also serves as the termination for the source-centered HV nMOSFET on N-epi/P-epi/N+substrate. The bottom P-epi also forms a double RESURF for the lateral HV nMOSFET which aids in the increase in doping and also in reducing the thickness of N-epi. Fig. 6.24 shows the cross-sections of the lateral HV nMOSFET on N-epi/P-epi/N+substrate with drain-centered and source-centered designs. The
drain-centered design with hybrid JTE shows effective performance demonstrating a BV of 530 V on N-epi/P-epi/N+substrate and a $R_{on,sp}$ of 6.81 m$\Omega \cdot$cm$^2$, as shown in Fig. 6.25.

Unlike the source-centered design on N-epi/N+substrate, the design on N-epi/P-epi/N+substrate has an additional electric field at the breakdown (D-D') between the N-epi/P-epi junction that needs to be terminated, as shown in Fig. 6.26a. The source-centered design without the P+isolation offers a BV of 175 V, as shown in Fig. 6.26c, due to its inability to terminate the electric field at the N-epi/P-epi junction. Although there is scope for further optimization, the usage of P+ isolation for source-centered design at the periphery significantly improved the BV up to

Figure 6.25: (a) Electric field profile across C-C' at the breakdown (b) Typical output characteristics and the extracted $R_{on,sp}$ at $V_{gs}$ of 25V and $V_{ds}$ of 0.1V is 6.81m$\Omega \cdot$cm$^2$; (c) Blocking characteristics measured at 25oC—BV = 530V at $V_{gs}$ of 0V.
480 V validating an effective termination, as shown in Fig. 6.26c. The $R_{on,sp}$ of both the devices remains similar at 6.85 and 6.75 mΩ·cm², as shown in Fig. 6.26b.

![Electric field profile across D-D' at the breakdown](image-a)

![Typical output characteristics and the extracted $R_{on,sp}$](image-b)

![Blocking voltages measured at 25°C](image-c)

**Figure 6.26:** (a) Electric field profile across D-D’ at the breakdown (b) Typical output characteristics and the extracted $R_{on,sp}$ at $V_{gs}$ of 25V and $V_{ds}$ of 0.1V for with and without P+ Isolation are 6.85mΩ·cm² and 6.75mΩ·cm² respectively (c) Blocking voltages measured at 25°C with and without P+ Isolation are 420V and 175V respectively at $V_{gs}$ of 0V.

Table.1 summarizes the sizes, the feasibility of the respective HV nMOSFETs for power IC integration, and the static characteristics of the devices. The HV nMOSFETs on the N-epi/P-epi/N+substrates are the ideal candidates for power IC integration as the epi stack offers isolation between the HV and LV segments. The $R_{on,sp}$ (chip) of the source-centered design is smaller when compared to that of the drain-centered design due to the significant reduction in the chip area as there is no requirement for edge termination.
6.5 Conclusions

This chapter demonstrated the lateral HV nMOSFETs with various edge termination and peripheral design architectures fabricated on a 6” N-epi/N+substrate and N-epi/P-epi/N+substrate for the development of HV SiC Power ICs. Based on the reported device architectures, an ideal lateral HV nMOSFET can be designed and used for power IC integration. The P+ Isolation that is intended for isolation between the voltage differential wells for the Power ICs effortlessly served as a termination to improve the breakdown voltage of the HV nMOSFETs.
References


CHAPTER 7: Low-Voltage (LV) Complementary Metal-Oxide-Semiconductor (CMOS) Development in 4H-SiC

7.1 Introduction

CMOS technology has emerged as a superior choice for power IC development when compared to JFET and BJT technologies. CMOS offers numerous advantages over JFET and BJT in terms of efficiency, integration, scalability, power dissipation, and reliability [1]-[8]. Here are a few technical details of why CMOS is considered a superior technology for power IC development compared to JFET and BJT.

*Higher Integration Density:*

CMOS technology enables higher integration density on a single chip compared to JFET and BJT. CMOS power ICs can integrate power devices, gate drivers, control circuitry, and other functional blocks on the same chip. This integration reduces interconnect parasitics and improves overall performance. In contrast, JFET and BJT technologies typically require separate components for power devices and control circuitry, leading to larger circuit sizes and increased parasitics [1]-[8].

*Lower Power Dissipation:*

CMOS power ICs exhibit lower power dissipation compared to JFET and BJT technologies. CMOS devices operate in a complementary manner, with both n-type and p-type transistors working together. This complementary operation reduces static power dissipation, resulting in improved energy efficiency[1]-[8]. In contrast, JFET and BJT devices may suffer from higher static power dissipation, limiting their overall efficiency.
**Scalability and Flexibility:**

CMOS technology offers excellent scalability and flexibility in design when compared to JFET and BJT technologies. CMOS power ICs can be easily scaled down in size, allowing for higher power density and increased integration. The ability to scale the technology enables the development of more advanced and efficient power ICs. Additionally, CMOS technology provides flexibility in design by allowing for the implementation of different power management topologies, such as buck, boost, and multi-level converters, to address diverse power conversion requirements [1]-[8].

In summary, CMOS technology offers significant advantages over JFET and BJT technologies in terms of higher integration density, lower power dissipation, scalability, flexibility, reliability, and manufacturing cost. These advantages have positioned CMOS as a superior choice for power IC development, enabling the realization of efficient, compact, and high-performance power electronic systems.

Very few groups have researched and reported the possibilities of the development of CMOS technology in 4H-SiC. The research into developing CMOS technology in 4H-SiC has been sluggish over the years with very few demonstrations. Despite the advancements in the material, process, and the demonstrated high-temperature capabilities of 4H-SiC, the lack of a standard CMOS process hindered the progress in realizing the power electronic IC applications. The first monolithic 4H-SiC IC was demonstrated based on an NMOS technology on 6H-SiC [9]. But, the 4H-SiC-based CMOS IC was first demonstrated by Cree based on the process flow of vertical power MOSFET [10]. Over the last decade, the University of Arkansas, Ozark Technologies, and Raytheon collaboratively demonstrated several 4H-SiC CMOS ICs for various applications [11]-
Apart from CMOS, the use of 4H-SiC all-NMOS [18], JFET [19], and BJT [20] technologies for IC demonstration has also been reported. This chapter reports the results and discusses the design of module processes implemented for CMOS development. The CMOS development (channel engineering for wells designs, gate oxide, and ohmic formation) has been conducted and fabricated on two different epi stacks: N-epi/N+ substrate, and N-epi/P-epi/N+ substrates. Since only the top N-epi layer plays a role in determining

**Figure 7.1:** Cross-section showing the LV NMOS and LV PMOS which are implemented by implanting the N+/P+ source/drain/bulk regions into P Well and N Well regions [17].
the electrical properties of the CMOS, the results from both the epi stacks have been integrated and reported in this chapter.

7.2 Well Designs

The NMOS and PMOS are implemented by implanting the N+/P+ source/drain/bulk regions into P Well and N Well regions as shown in Fig. 7.1. The P Well and N Well regions are designed to precisely control the current through the channel. The peak doping of P Well and N Well are about $2 \times 10^{18} \text{ cm}^{-3} – 3 \times 10^{18} \text{ cm}^{-3}$. Channel engineering was performed by implementing both accumulation (accu.) and inversion (inv.) channels in this work. The accumulation channel implements a thin sheet of N/P layer (N layer for NMOS, P layer for PMOS) as shown in Figs. 7.2 and 7.4. This thin sheet affects the band near the surface reducing the flat band voltage and consequently decreasing the threshold voltage [21]. The thin sheet for forming the accumulation channel is either implemented by implantation or by epitaxy. The gate oxide condition (#2), which is 50nm targeted deposited oxide discussed in section 7.3 was used for the Well designs reported in this section.

7.2.1 P Well design

Since the LV NMOS in this work is integrated with the HV power NMOSFET, the P Well design for LV NMOS is similar to the HV Power MOSFET. The P Well design for NMOS is designed to target a threshold voltage of 6V. As [22] reports, the accumulation channel for the NMOS offers a better trade-off between threshold voltage and mobility, and thus the P Well designs in this work use only an accumulation mode channel. The implantation profiles of the P Wells designed for this work are shown in Fig. 7.2. The accumulation channel for the P Well in this work
is formed by utilizing the epitaxial doping of the N-epi layer from the epi stacks. Hence, one of the designs has a channel doping of $2.5 \times 10^{16}$ cm$^{-3}$ (blue curve in Fig. 7.2), and the other with $6.5 \times 10^{16}$ cm$^{-3}$ (red curve in Fig. 7.2). Based on the increased channel doping of $6.5 \times 10^{16}$ cm$^{-3}$, the channel depth is reduced by increasing the dose of the P Well implantation to target a similar threshold voltage as $2.5 \times 10^{16}$ cm$^{-3}$.

After fabrication and measurement, the extracted threshold voltages of both the designs using the linear extrapolation method remain the same at ~6.2V as shown in Fig. 7.3. These threshold voltage results demonstrate an accurate and precise design of P Well that can be implemented to design LV NMOS and HV Power MOSFET simultaneously.

**Figure 7.2**: Implantation profiles of P Well designed for the implementation of LV NMOS using SRIM with channel doping of $2.5 \times 10^{16}$ cm$^{-3}$ and channel doping of $6.5 \times 10^{16}$ cm$^{-3}$.
Figure 7.3: The measured transfer characteristics of the LV NMOS of both the designs show a similar Vth of about 6.2V

7.2.2 N Well Design

The design of N Well is extremely critical for the optimum performance of PMOS. Since the design of PMOS is fairly new and unexplored, several N Well designs with both inversion and accumulation channels were implemented. Two inversion mode channel designs with different doping concentrations and a single accumulation mode channel design were implemented. The doping concentrations at the surface of the inversion channel are varied, one with channel doping of $3 \times 10^{16}$ cm$^{-3}$ (brown curve in Fig. 7.4) and another with $6.5 \times 10^{16}$ cm$^{-3}$ (purple curve in Fig. 7.4). The surface doping concentration of the accumulation channel is about $2 \times 10^{17}$ cm$^{-3}$ (blue curve in Fig. 7.4). The overlapped implantation profiles of all the three N Well channel design variations is shown in Fig. 7.4. The extracted threshold voltages of both the inversion channels
Figure 7.4: Implantation profiles of N Well designed for the implementation of LV PMOS using SRIM. Three different N Well profiles (accumulation (blue curve) and inversion channels (green and red curves) were implemented.

Figure 7.5: Measured transfer characteristics of the LV PMOS in which the accumulation channel offers the lowest $V_{th}$. 

$V_{th} = 11.13\text{V}$

$V_{th} = 11.08\text{V}$

$V_{th} = 8.80\text{V}$
exhibit similar voltages at about ~11V as shown in Fig 7.5. However, on the other hand, the accumulation mode channel with a channel doping concentration of 2 x 10^{17} cm^{-3} demonstrated a significantly improved threshold voltage of 8.8V (Fig. 7.5). Implementing a thin layer of P-layer at the surface reduced the threshold voltage due to the effects on the band bending near the inversion layer of the surface.

### 7.3 Gate oxide development

A single gate oxide process was used in this work to achieve maximum electron and hole channel mobilities and superior dielectric qualities. Several gate oxide recipes comprising variations in formation methods (thermal oxide vs deposited oxides), post-oxidation annealing timings, and oxide thicknesses were implemented. Table. 7.1 summarizes the gate oxide recipes implemented in this work.

**Table 7.1: Summary of the gate oxide split conditions with formation processes, thickness, and POA conditions**

<table>
<thead>
<tr>
<th>Condition #</th>
<th>Gate Oxide formation</th>
<th>Target thickness</th>
<th>Post-Oxidation Anneal</th>
<th>POA - 1</th>
<th>POA – 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Thermal oxidation</td>
<td>50 nm</td>
<td>800 °C for 180 min</td>
<td>1250 °C diluted N₂O, 20% N₂, 180 min</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Deposited</td>
<td>50 nm</td>
<td>N/A</td>
<td>1250 °C diluted N₂O, 20% N₂, 180 min</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Deposited</td>
<td>25 nm</td>
<td>N/A</td>
<td>1250 °C diluted N₂O, 20% N₂, 90 min</td>
<td></td>
</tr>
</tbody>
</table>
Condition #1 is a thermally grown gate oxide recipe with a target thickness of 50nm. There are two post-oxidation anneals (POA’s) performed to improve the quality of oxide. The POA-1 was performed at 800 °C for 180min followed by a POA-2 for 180min at 1250 °C in diluted N₂O and 20% N₂. Conditions #2 and #3 are deposited gate oxides with a target thickness of 50nm and 25nm, respectively. Only POA-2 was performed for conditions #2 and #3. A thinner gate oxide recipe was designed to see the impact on mobility, threshold voltage, and gate-source breakdown.

![Graph](image)

**Figure 7.6:** (a) Measured field effect mobility curves of the LV NMOS extracted from 200 µm x 200 µm FATFET (b) Field effect electron channel mobility variation for the devices with different gate oxide conditions. The box plots show the minimal variation of electron mobility across the wafers.

The field effect mobility curves of electrons and holes, along with their corresponding channel mobility variations across the wafer, were summarized in Figures 7.6 and 7.7. The field-effect channel mobilities were extracted from 200 µm x 200 µm FATFETs. In Condition #1, corresponding to the thermally grown gate oxide recipe, the electron channel mobility exhibited a lower value of 18 cm²/V-s compared to the deposited gate oxide recipes, which showed approximately 20 cm²/V-s as depicted in Figure 7.6. However, the hole channel mobilities remained similar at around 9 cm²/V-s, irrespective of whether the oxide was thermally grown or
deposited, as shown in Figure 7.7. As expected, gate oxide recipes with different thicknesses (Conditions #2 and #3) demonstrated similar electron and hole channel mobilities.

![Image of measured field effect mobility curves](chart1.png)

**Figure 7.7:** (a) Measured field effect mobility curves of the LV PMOS extracted from 200 µm x 200 µm FATFET (b) Field effect electron channel mobility variation for the devices with different gate oxide conditions. The box plots show the minimal variation of electron mobility across the wafers.

The threshold voltage variations of NMOS and PMOS for all three gate oxide conditions were also extracted as shown in Figs. 7.8 and 7.9. As observed in Fig. 7.8, the thermally grown oxide also affects the threshold voltage of the NMOS. Coming to the PMOS, as shown in Fig. 7.9, there is no significant difference in the threshold voltages of PMOS for either thermally grown or deposited oxides. This reduction in mobility and increase in threshold voltage for the thermally grown oxide can be attributed to the large Density of interface (Dit) states when compared to the deposited oxide conditions. As expected, the thinner gate oxide recipes offer lower threshold voltages in the case of both NMOS and PMOS due to an increase in the capacitance of the oxide leading to an increase in the drain current of the device (Figs. 7.8 and 7.9).
The dielectric breakdown of NMOS and PMOS was also extracted by measuring the gate-source breakdown as shown in Figs. 7.10. The gate-source breakdown of both NMOS and PMOS for 50nm targeted gate oxide conditions (#1 and #2) showed a very low leakage current (1pA at Vgs of 30V) demonstrating a high breakdown field. On the other hand, the thinner gate oxide

Figure 7.8: (a) Measured transfer characteristics of the LV NMOS extracted from 20 µm x 20 µm device for the three different gate oxide conditions (b) Vth variation for the NMOS devices and the box plots show the minimal variation in Vth across the wafers

Figure 7.9: (a) Measured transfer characteristics of the LV NMOS extracted from 20 µm x 20 µm device for the three different gate oxide conditions (b) Vth variation for the NMOS devices and the box plots show the minimal variation in Vth across the wafers
condition (#3) also showed reasonably low leakage of about 0.1nA at Vgs of 20V. An extensive BTI analysis was conducted on these gate oxide conditions which are reported in [23] demonstrating a safe and reliable operation of devices with an assured Vgs up to 30V for thicker gate oxide (conditions #1 and #2) and up to Vgs of 20V for thinner gate oxide (condition #3). As reported in section 7.2, the P Well condition with accumulation channel doping of $2.5 \times 10^{16}$ cm$^{-3}$ was used for gate oxide condition #1, and channel doping of $6.5 \times 10^{16}$ cm$^{-3}$ for gate oxide conditions #2 and #3 to report the performances of NMOS. For the PMOS, N Well with inversion mode with a channel doping of $2.5 \times 10^{16}$ cm$^{-3}$ was used.

![Graphs showing gate-source current vs. gate-source voltage for NMOS and PMOS](image)

**Figure 7.10:** (a) Gate-source dielectric breakdown of NMOS for all three gate oxide conditions; the layout view of the NMOS is also shown in the inset (b) Gate-source dielectric breakdown of PMOS for all three gate oxide conditions; The layout view of the PMOS is also shown in the inset

### 7.4 Ohmic contact development

One of the most critical issues that can conceivably limit the device's performance is contact resistance. It is highly imperative to achieve reliable and low-resistance ohmic contacts. Due to the wide bandgap of 4H-SiC, the barrier heights are large to form the ohmic contacts with
work functions typically at 4 eV for the n-type and about 7 eV for the p-type. Achieving the lowest possible p-type contact resistance is still a challenge and extremely important for the development of CMOS technology in 4H-SiC. Separate ohmic contact metals with separate processes for n-type, and p-type ohmic contacts on 4H-SiC can yield better ohmic contacts but separate approaches complicate the process flow requiring dual metals and dual annealing temperatures. Alternatively, being able to use the same contact material for both p-type and n-type 4H-SiC will simplify the processing scheme. Nickel (Ni) has been well established as the ideal ohmic metal for the formation of n-type contact from the extensive research efforts in optimizing the traditional vertical power nMOSFETs by our group and other groups as well.

We report two important research aspects in an attempt to improve the contact resistance of the p-type ohmic. The first one is to increase the surface doping of the P+ regions with Ni as ohmic metal. Ni usually forms rectifying contact to p-type, but due to the increase in doping density in the P+ region at the surface, reduces the barrier width at the interface, increasing the tunneling current and leading to a better formation of ohmic contact. Fig. 7.11 shows the P+ profiles with lower and higher doses at the surface. As intended, the increase in the dose of the P+ region significantly reduced the specific contact resistance from $4.31 \times 10^{-1}$ ohm-cm$^2$ to $1.61 \times 10^{-3}$ ohm-cm$^2$ as shown in Fig. 7.12.

The second aspect is exploring different metal stacks with Titanium (Ti) and Ni combinations. Ti was added to Ni to form carbides and silicides and consequently reducing the carbon clusters at the surface. Three conditions were designed with variations in the metal stacks as shown in Table 7.2 to form better ohmic contacts. The thickness of Ni metal in the three conditions is kept constant at 1000 Å.
Figure 7.12: Extracted contact resistance from the P+ TLM for the lower and higher-dosed P+ regions with high-dosed P+ showing significant reduction in the specific contact resistance from $4.31 \times 10^{-1} \text{ ohm-cm}^2$ to $1.61 \times 10^{-3} \text{ ohm-cm}^2$
Table 7.2: Ohmic contact formation conditions for better p-type contact resistance

<table>
<thead>
<tr>
<th>Condition #</th>
<th>Metal Stack (4H-SiC/…)</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ni</td>
<td>1000 Å</td>
</tr>
<tr>
<td>2</td>
<td>Ti/Ni</td>
<td>200 Å /1000 Å</td>
</tr>
<tr>
<td>3</td>
<td>Ni/Ti/Ni</td>
<td>200 Å /200 Å /1000 Å</td>
</tr>
</tbody>
</table>

The extracted n-type and p-type contact resistances from the cTLM structures were summarized in Figs. 7.13. Condition #1 which uses the single Ni (1000 Å) metal offers the lowest possible contact resistance for both N-type and P-type regions. The anticipated formation of carbides and silicides with Ti (conditions #2 and #3) doesn’t seem to be conceived leading to an adequate contact resistance for both n-type and p-type contacts. Varying the annealing temperatures for conditions #2 and #3 can be further explored to form better n-type and p-type contacts and target the anticipated lower contact resistance.

Figure 7.13: (a) Extracted contact resistances of the N+ region from the circular TLM structures for the three different metal stack conditions. Ni metal offers the lowest contact resistance of $3.47 \times 10^{-3} \text{ ohm-cm}^2$ (b) Extracted contact resistances of the P+ region from the circular TLM structures for the three different metal stack conditions. Ni metal offers the lowest contact resistance of $1.61 \times 10^{-3} \text{ ohm-cm}^2$
7.5 Conclusions

A detailed examination encompassing the fabrication, design, and crucial module process advancements specific to complementary metal-oxide-semiconductor (CMOS) technology for the development of 4H-SiC Power Integrated Circuits (ICs) has been extensively documented in this chapter. The elucidated CMOS technology framework serves as a foundation for the forthcoming realization of high-voltage (HV) power electronic circuit applications, notably the half-bridge power driver and a buck converter, within the scope of this project. Noteworthy progress has been achieved in establishing an operational PMOS (p-channel metal-oxide-semiconductor) component. However, opportunities for further advancements remain in terms of enhancing the mobility, threshold voltage, and contact resistance characteristics of the PMOS device. Addressing these areas of improvement holds significant potential for elevating the overall performance and efficacy of the CMOS-based 4H-SiC Power ICs, paving the way for enhanced power electronic applications.

7.6 References


CHAPTER 8: Demonstration of 4H-SiC Digital CMOS Integrated Circuits (ICs) for Emerging High-Temperature Power IC Applications

8.1 Introduction

The inherent superior material properties of 4H-SiC are responsible for its exceptional candidacy for high-power and high-temperature operation. Any temperatures beyond the standard commercial temperature (0 °C to +85 °C) or the military specification temperature standard (~55 °C to +125 °C) are considered extreme/high temperatures [1]. One of the major challenges in high-temperature power IC technology is the reliability of the materials and devices. Traditional silicon-based ICs have limited temperature tolerance due to the degradation of materials and increased leakage currents at elevated temperatures. To address these challenges, researchers have explored alternative materials such as silicon carbide (4H-SiC) and gallium nitride (GaN) for high-temperature power devices. These wide-bandgap materials offer superior thermal stability, higher breakdown voltages, and lower conduction losses, enabling efficient power conversion at high temperatures [1][2].

The current generation power electronic technologies, predominantly Bulk Silicon and Silicon-On-Insulator (SOI) technologies have limitations in their operational temperatures [2]. Based on the theoretical limits, Si-based ICs are rated 150 °C and are not operational beyond 200 °C due to leakage and reliability issues. Although SOI technology offers relief up to 300 °C, with the insulated region, it also fails beyond 300 °C [2]. The wide bandgap (4H-SiC) based electronics can solve this issue and has the capability to address the application space for extreme environments. Fig. 8.1 condenses the power capabilities and peak ambient temperatures of various
HT power electronic applications [2]-[5]. A few significant HT applications and the scope for the 4H-SiC power electronic systems are discussed here [2][3][4].

**Automotive Electrical Systems**

In automotive electrical systems, there is a need for a power requirement of >10kW and temperatures <300 °C in the electrical development (PMAD) systems. Also, in the on-cylinder and exhaust pipes where the temperature goes up to 600 °C, 4H-SiC-based power ICs can be an effective solution.

**Turbine Engine Control Electronics**

The requirement of temperatures up to 600 °C in sensor, telemetry, and control circuitry can be addressed by 4H-SiC-based ICs. Not only that but the current generation electrical actuation systems and 600 °C requirements can be fulfilled.

**Spacecraft and Venus exploration**

The power management modules in the spacecraft can be performance enhanced with the 4H-SiC-based Power ICs where the power levels are >1kW. In the significant Venus and mercury exploration where temperatures go as high as 550 °C, 4H-SiC technology has the potential to address the requirement for reliable and rugged electronics operation.

**Drilling Instrumentation and Monitoring**

Telemetry electronics for oil, gas, and geothermal drilling technologies where temperature requirement is up to 600 °C can be resolved using 4H-SiC-based electronics. Also due to the extended hours of operation, highly reliable monitoring electronics can be accomplished using 4H-SiC.
4H-SiC-based high-temperature electronics may have potential demand in emerging applications, in addition to their contemporary cases. Given the maturity and economical aspect of the Bulk Si and SOI technologies, it will be unlikely that 4H-SiC-based electronics are needed below 300 °C. Nevertheless, even at operating temperatures below 300 °C, as outlined in section 1.2.2, the authors acknowledge that 4H-SiC possesses the potential to serve as a promising solution for power IC (multiple power integrated functions onto a single chip) applications where the power levels exceed 1 kW due to the low specific on-resistance [6] when compared to its Si counterparts.
Although the ultimate objective of this work is to develop 4H-SiC-based high-voltage (HV) power ICs [7], this work also focused on evaluating the operation of CMOS ICs at extreme temperatures. Hence this chapter covers the characterization and operation of digital CMOS ICs up to 400 °C by reporting the packaging flow, assembly process, materials employed, and challenges encountered during HT measurements of the ICs.

8.2 Packaging and HT measurement system

Fig. 8.2 depicts the 6-inch wafer of the reported ICs and other test structures, with the IC dimensions measuring 10 mm x 10 mm. The IC was sintered, wire bonded, and encapsulated inside an 84 CQFJ package. The package model was adhered to with 84 pads, each with dimensions of 200 μm x 200 μm. The Kyocera A-440 material used for the 1.15-inch x 1.15-inch 84-pin CQFJ IC package contains Alumina, Tungsten, and Molybdenum, with melting points exceeding 300 °C.
Figure 8.3: Top view and cross-section views of the 4H-SiC IC package mounted onto the test board PCB

Figure 8.4: Brass and ceramic fixture used on top of the hotplate for mounting the test board PCB containing the 4H-SiC IC package

Figure 8.5: Side view of the 4H-SiC IC package on the test board PCB mounted to the brass fixture atop the hot plate
Similarly, the package leads were Alloy 42 (Fe-Ni-Co alloy), which has a melting point greater than 300 °C. The Namics XH9890-6S Ag-sinter paste used for die attachment has a melting point > 900 °C after sintering, while the encapsulant was Wacker SEMICOSIL 915 HT silicone gel rated for ~250 °C. After packaging the 4H-SiC ICs, a socket-less PCB test board was designed due to the unavailability of off-the-shelf IC package sockets rated for >300 °C. The IC package was soldered using solder paste to the PCB pads located around the cut-out region of the test board PCB as depicted in Fig. 8.3. The PCB for the test board is composed of Isola polyimide, which has a Tg of over 250 °C to endure the high temperature emanating from the hotplate throughout the measurements. The test setup was designed to establish thermal contact only with the 4H-SiC IC package. A thermal conduction method was adopted to gauge the 4H-SiC packaged IC at elevated temperatures due to its comparative simplicity and compatibility with the 4H-SiC packed ICs. The test board PCB was mounted on a brass plate utilizing ceramic standoffs. A brass finger heating block established physical contact with the package's backside to allow for thermal conduction to apply > 300 °C to the 4H-SiC IC as shown in Fig. 8.4. A small notch was carved into the top of the brass finger to accommodate a thermocouple to more accurately monitor the temperature of the 4H-SiC IC package, as the thermal resistance of the test setup will cause a temperature difference between the set point temperature of the hotplate and the actual temperature at the backside of the 4H-SiC IC package. As shown in Fig. 8.5, the IKA hot plate has a ceramic glass plate that can deliver a temperature up to 500 °C and provide electrical isolation during the measurements. Fig. 8.6 displays the entire custom-built HT IC measurement setup, including a hot plate, brass heating plate and finger, ceramic stand-offs, thermocouple, thermometer, HT PCB test board, IC chip, and oscilloscope. At the maximum set point temperature of 500 °C, the thermocouple at the base of the IC package reads 450 °C.
Prior to packaging, probe testing was conducted on the (width/length) 10μm /1μm and 50μm /1μm sized NMOS and PMOS, respectively, at both 25 °C and 300 °C. The output and transfer characteristics of NMOS and PMOS are depicted in Figs. 8.7 and 8.8. A negative threshold shift was observed for both NMOS and PMOS, which can be attributed to the reduction in the voltage required for surface band bending (2Φf) for strong inversion significant increase in the intrinsic 4H-SiC carrier concentration (ni) from room temperature to 300 °C and also the change in the charge (QtI) adhered in the interface states [8]. The marked improvement in the PMOS current at 300 °C is due to the decrease in the sheet resistance of the p-regions from 1.7kΩ/sq at 25 °C to 0.2kΩ/sq at 200 °C extracted from a TLM structure.
Figure 8.7: (a) Output and (b) transfer characteristics of the W/L (10μm /1μm) sized NMOS measured at 25 °C and 300 °C

Figure 8.8: (a) Output and (b) transfer characteristics of the W/L (10μm /1μm) sized NMOS measured at 25 °C and 300 °C

8.4 Ring oscillator

The schematic of the fabricated ring oscillator is presented in Fig. 8.9. The ring oscillator is composed of 5 inverter stages, each made of NMOS and PMOS with W/L dimensions of 0.7
μm/2 μm, and 0.7 μm/7.2 μm, respectively. The disparity in the W/L for the NMOS and PMOS are to account for the mobility differences to ensure the delay times match. The top view of the layout and a close-up view of the ring oscillator comprising the 5 stages can also be viewed in Fig. 8.9. Following the ring oscillator, a CMOS buffer circuit comprising 10 inverter stages with a fan-out ratio of 2 was incorporated to drive the parasitic load capacitance.

**Figure 8.9:** Schematic of the 5-stage ring oscillator, each made of NMOS and PMOS with W/L (width/length) dimensions of 0.7 μm/2 μm, and 0.7 μm/7.2 μm respectively; top view of the ring oscillator layout and a close-up view of the gds layout of the 5-stages inverter

**On-wafer vs Packaged IC measurement:**

The ring oscillators were subject to characterization both before and after packaging, in which their operating frequency at a supply voltage of 25V and a temperature of 25 °C was found to be approximately 0.7 MHz in both cases. However, the packaging measurements revealed a
significant improvement in the oscillating waveforms, resulting in a cleaner output as evidenced by Fig. 8.10. This improvement can be attributed to the reduction in parasitic inductance and capacitance due to the IC package.

**Figure 8.10:** Operation of the on-wafer and packaged characterizations of the ring oscillator at a supply voltage of 25V; the packaged measurements show cleaner waveforms due to the reduction in parasitic inductances and capacitances

**HT measurement:**

The packaged ring oscillator was characterized operating at supply voltages of 20 V and 25 V at temperatures ranging from 25 °C to 450 °C. The characterization measurements were taken after a 30-minute delay at each temperature set point to attain equilibrium. Fig. 8.11 demonstrates the observed variations in the ring oscillator’s operating frequency regarding the temperature and supply voltage. As shown, the operating frequency of the ring oscillator increases with the increase in the supply voltage. At a supply voltage of 25 V, the maximum operating frequency measured was 1.38 MHz at a temperature of 275 °C, with the minimum operating frequency observed at 0.69 MHz at 25 °C, and the frequency measured at 450 °C was 1.1 MHz. The initial increase and then decrease in the operating frequency over the temperature range can be explained by the peak field effect mobility behavior with temperature. This mobility behavioral pattern with temperature
increase in 4H-4H-SiC was experimentally reported in [9] where the field effect mobility peaks at 167 °C abiding by the Coulomb scattering and then decreases with the further increase in the temperature suggesting the impact of bulk phonon scattering.

8.5 CMOS Inverter

Fig. 8.12 shows the schematic, layout top view, and closeup view of the CMOS inverter. The inverter is constructed with an LV NMOS and PMOS of W/L sizes of 0.7 μm/0.5 μm and 3.5 μm/0.5 μm, respectively. The transistors are once again sized to match the mobility discrepancy between NMOS and PMOS. Similar to the ring oscillator, the inverter circuit was followed by a CMOS buffer with 10 inverter stages and a fan-out ratio of 2.
In order to perform the inverter circuit electrical tests, control input from a function generator and a level-shifter board were needed to apply the appropriate input voltage signals to the inverter. The level-shifter output of -3V to 22V, 1kHz pulse signal acts as a control input to the inverter. HT measurements of the inverter were performed up to 400 °C. As shown in Fig. 8.13, the output waveform (red curve) shows a proper dynamic operation of the inverter across all temperature ranges. The negative magnitude in the input square wave is because of the level-shifter board that has a maximum Vpp of 25 V, and a maximum Vee that was below 0V (-3V). However, the input wave and the inverter output magnitude were determined solely by the applied external DC power supply voltage which was 22V.

Figure 8.12: Schematic of the CMOS inverter, each made of NMOS and PMOS with W/L (width/length) dimensions of 0.7 μm/0.5 μm, and 3.5 μm/0.5 μm respectively; top view and a close-up view of the gds layout CMOS inverter is also shown.
Figure 8.13: Dynamic operation of the CMOS inverter at temperatures ranging from 25 °C to 400 °C; Stable operation of the inverter can be observed at all temperature ratings

8.6 Physical Analysis for Failure

The primary challenge of the HT package-level test setup focuses on the interconnect between IC package leads and the PCB test board pads. This is because no other failures were observed within the IC package itself, including the insulating materials, the chip attachment, and the wire bonds. The solder joint, which attaches the IC package to the PCB, was identified as the weak point in the HT package-level test setup. The detachment of the IC package from the test board PCB occurs once the temperature of the SAC solder (rated 200°C) joint exceeds the liquidus
temperature. It was observed that the polyimide-based test board PCB continues to provide robust performance during the HT electrical tests while evaluating the packaged IC circuits.

### 8.7 Conclusions

In conclusion, this chapter discusses the successful demonstration of digital CMOS ICs in 4H-SiC at extreme temperatures up to 450 °C. The packaging flow, design of the HT measurement system, and failure analysis have also been discussed. The HT operation of circuits showed no signs of operational failures from a process or packaging standpoint up to 400 °C demonstrating the potentiality of 4H-SiC for HT applications. This successful performance at extreme temperatures further confirms the potential of silicon carbide (4H-SiC) as a promising material for the development of high-temperature electronics. Overall, the reported designs and results serve as a foundation for the future realization of HV and HT power ICs.

### 8.8 References


CHAPTER 9: Summary and Future Work

9.1 Summary

This dissertation presents a comprehensive exploration of the design and development of SMART Power ICs in 4H-SiC. It consists of several chapters, with each chapter addressing specific aspects of SMART Power IC technology as summarized below.

In conclusion, Chapter 2 offers an in-depth exploration of drift layer design in wide bandgap semiconductors, specifically focusing on 4H-SiC. The comprehensive trade-off analysis conducted in this chapter encompasses critical factors such as breakdown voltage assessment, impact ionization coefficients, critical electric field dependence on doping concentration, and the importance of incomplete ionization for specific on-resistance considerations. The insights gained from this analysis empower researchers to make informed decisions when optimizing the non-punch-through (NPT) drift layer design for wide bandgap semiconductors. Furthermore, the chapter delves into the drift layer design for unipolar power devices within the voltage range of 600V to 25kV, with particular emphasis on 4H-SiC. Both NPT and punch-through (PT) designs are explored, and simplified generalized equations are derived using mathematical power series curve fitting techniques. These equations serve as invaluable design guidelines, offering profound insights into selecting appropriate drift layer architectures based on the desired voltage rating.

Chapter 3 serves as a valuable process document, guiding design and fabrication teams through the complete manufacturing run of the technology. Key considerations such as starting materials, fabrication process flow, device designs, and high-voltage and low-voltage integration are highlighted, accompanied by valuable simulated and experimental information to ensure successful design outcomes.
Chapter 4 focused on the development of HV Lateral MOSFETs and diodes in 4H-SiC, specifically tailored for integration within power ICs. The development process includes simulations and in-depth analysis of experimental results. The chapter details the rigorous experimentation performed on N-epi/N+ substrates and N-epi/P-epi/N+ substrates, leading to designing the best-in-class BV-$R_{\text{on,sp}}$ trade-off performances. Not only that the devices have the best trade-off performance, but they are also high current rated which demonstrates the design and edge termination efficiency. A notable accomplishment is the demonstration of an enhanced design architecture (Gen 2) for lateral devices in 4H-SiC which addresses all the prominent surface field management issues in lateral devices making it a robust and reliable design.

Chapter 5 delved into high-voltage isolation techniques crucial for ensuring the safety, reliability, and proper functioning of electronic systems. Various techniques to prevent electrical leakage and isolate sensitive circuitry from damaging voltage levels are discussed, with specific emphasis on junction isolation using the P+ Isolation junction implemented by channeling implantation. The effectiveness of these techniques is supported by electrical measurements. Furthermore, the interlayer dielectric (ILD) voltage-blocking capability for metal-to-metal insulation between different voltage potentials is addressed, evaluating the ILD blocking capabilities between metals.

In Chapter 6, an extensive study on peripheral and edge termination techniques for lateral power devices is presented. Leveraging 2D TCAD simulations, techniques are designed to control and distribute the electric field at the edges of lateral devices, resulting in improved breakdown voltage and reliable operation. The significance of layout techniques is highlighted, demonstrating how lateral device layout techniques eliminate the need for edge termination while maintaining comparable static performances as the ones with edge termination.
Chapter 7 focused on the design of module processes for the development of CMOS. Channel engineering techniques are applied, optimizing designs with accumulation and inversion mode channels. Multiple gate oxide recipes are developed to target maximum channel mobilities of both electrons and holes. Efforts are dedicated to enhancing CMOS performance through optimized ohmic contacts, including the pursuit of metal contacts for the simultaneous formation of n-type and p-type ohmic contacts.

In Chapter 8, the potential scope for high-temperature (HT) integrated circuits (ICs) in 4H-SiC is explored through a comprehensive literature survey. Building upon the CMOS technology efforts discussed in Chapter 7, the chapter showcases the performance of CMOS ICs, justifying the potential of the developed technology. The operation of digital CMOS ICs at extreme temperatures up to 400°C is evaluated, covering packaging flow, assembly process, materials employed, and challenges encountered during HT measurements. This successful performance of CMOS ICs at extreme temperatures further confirms and validates the potential of silicon carbide (4H-SiC) as a promising material for the development of high-temperature electronics.

### 9.2 Future work

In light of the exceptional performance exhibited by high-voltage (HV) lateral MOSFETs, there remains an opportunity for further enhancement through the implementation of innovative gate oxide recipes. By incorporating these advancements, the performance of 4H-SiC lateral MOSFETs can be elevated to a level comparable to that of 4H-SiC vertical MOSFETs. Consequently, 4H-SiC lateral MOSFETs can emerge as formidable contenders in the 400-600V voltage range, competing with gallium nitride high-electron-mobility transistors (HEMTs) in terms of specific on-resistance, breakdown voltage, HT performance, and reliability. This, in turn,
broadens the prospects for widespread adoption of 4H-SiC lateral MOSFETs in various applications.

While the developed complementary metal-oxide-semiconductor (CMOS) technology is noteworthy, there exists potential for further enhancement of the PMOS performance to bridge the gap with the NMOS performance in terms of channel mobility and threshold voltage. By narrowing this performance disparity, designers are afforded greater flexibility in IC design, enabling the realization of more versatile and efficient electronic systems.

Given the current maturity level of power IC technology and the substantial room for advancements, it is prudent to explore alternative integration approaches, such as combining vertical MOSFETs with CMOS technology. This avenue presents an opportunity to delve deeper into the performance and economic aspects of power ICs, thereby driving progress in this field. Moreover, investigating the integration of power ICs on different substrate options, such as N-epi/N+ substrates or High Purity Semi-Insulating (HPSI) substrates, holds potential for significant advancements in the development of power ICs based on 4H-SiC. By exploring these integration techniques, new pathways can be forged to enhance the capabilities and applications of 4H-SiC-based power ICs.